Test 1 will be Tuesday, Oct. 9, in class. It will be closed book and notes, except for one 8.5" x 11" sheet of paper (front and back) with notes. Review topics for Test 1 are:

Chapter 1.
Basic structure and functional units of a computer
Functional units: Input, CPU, Memory, Output, System bus
CPU components: control unit, ALU, regs., internal CPU interconnection
History: Computer Generations: 1st (vacuum tubes), 2nd (transistors, early operating systems, and high-level programming languages), 3rd (small and medium scale integrated circuits), 4th (large and very large scale integrated circuits and microprocessors)
Moore's law, von Neumann model, Instruction/Machine cycle
Programming Languages: High-level language, Assembly Language, and Machine Language
Computer Level Hierarchy

Chapter 2.
Unsigned binary numbers
Conversion between base 10, base 2, and base 16
Signed number representation: sign bit and magnitude, one's complement, two's complement
Addition and subtraction of signed and unsigned numbers
Overflow in integer arithmetic
Booth's Algorithm for integer multiplication
Floating-point Representation: 32-bit and 64-bit IEEE 754 standard and special values
Addition and multiplication of floating-point numbers
Character Representations: Binary-Coded Decimal (BCD), EBCDIC, ASCII, Unicode
Error Detection and Correction: cyclic-redundancy check (CRC), Hamming Code, Reed-Soloman

Chapter 3 and Appendix 3A on Karnaugh maps. (SKIP SUBSECTION 3.6.6)
Truth tables for the gates
Boolean algebra notations: sum-of-products
Combinational circuit design (no memory): 1) determine truth table for function, 2) using Karnaugh/K-maps to get minimized sum-of-products function, 3) draw implementation of minimized function (using gates)
Common combinational circuits: decoder, multiplexer (MUX), 1-bit Adders (half and full), ripple-carry adder, faster (2-bit) carry-lookahead adders,
Number of gate delays for a circuit.
Complexity number of a circuit (# of gates + # inputs to gates)
Sequential Circuits (1-bit memory): SR latch - know how it remembers (two stable states, etc.), know how it changes states;
Gated/Clocked D latches. Master-slave D Flip Flop; their characteristic tables
Timing diagrams for latches and Flip Flops
Register file - design and usage
Square-memory implementation of large memories - understand (1) how the two level decoding of an address reduces the overhead for decoding, (2) how the tri-state buffers eliminate the need for MUXs, and (3) how a single-port RAM memory and two-level decoding reduces the wires to the memory chip