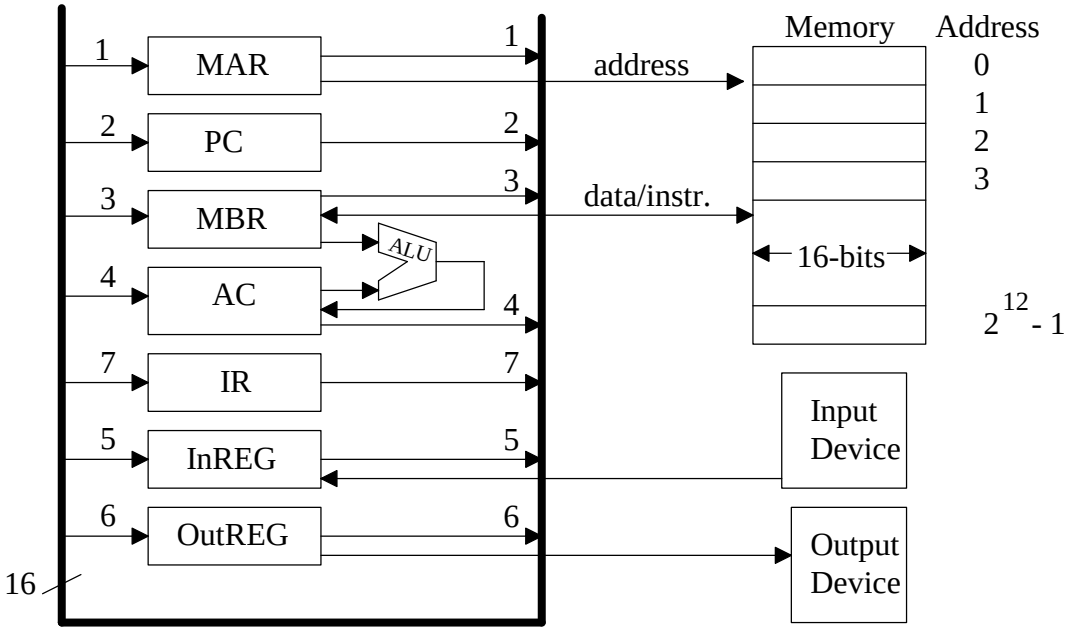
# Corrections to the Text

**In Figure 4.9** (the datapath in MARIE) it bothers me that the data into and out of the Main Memory comes from the Bus and not the MBR. I would prefer the following figure:

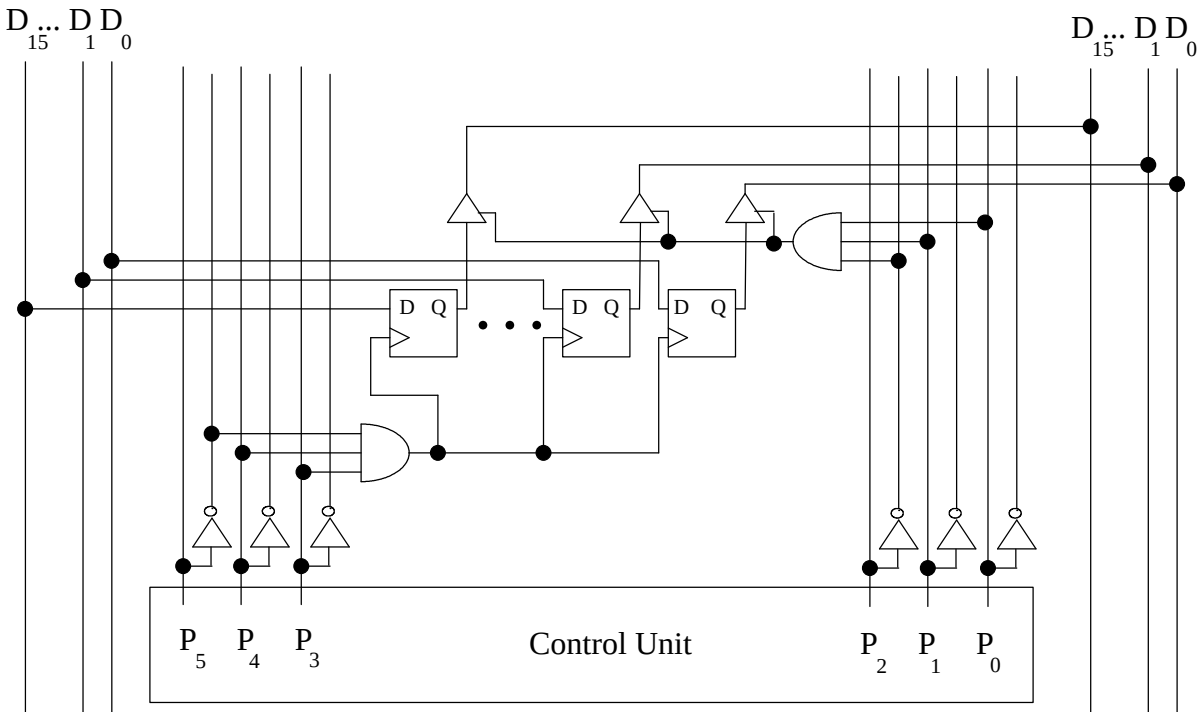
Revised Figure 4.9 Datapath in MARIE




Additionally, Figure 4.9 does NOT support the RTN of PC ← PC + 1, but that is a relatively minor issue.

**Figure 4.15** seems to have numerous mistakes, especially related to connections of Flip-Flops to the Bus ($D_{15}$-$D_0$). First, recall that seven registers are connected similarly to the Bus ($D_{15}$-$D_0$). When the (upper) AND gates from the MBR register are outputting to the bus, the remaining registers would be outputting 0 to the same wires causing the values to be garbled. Similarly, when storing to a different register (other than the MBR), the D-input of the FFs will all be 0. Thus, clearing its contents. A revised Figure 4.15 is as follows:

Revised Figure 4.15 Connection of MARIE's MBR to Datapath



**In Figure 4.14 (abc)**, the "(Decode IR[15-12])" occurs concurrently with the MAR ← IR[11-0], so I put "(Decode IR[15-12])" in the "Step" column instead of just "Decode". Additionally, I've added number to the steps in these table for later reference at the end of subsection 4.13.1.

## Revised Figure 4.14 (a) LOAD 104

| Step | Step # | RTN | PC | IR | MAR | MBR | AC |
|---|---|---|---|---|---|---|---|
| (initial values) | | | 100 | | | | |
| Fetch | $T_0$ | MAR ← PC | 100 | | 100 | | |
| | $T_1$ | MBR ← M[MAR] | 100 | | 100 | 1104 | |
| | $T_2$ | IR ← MBR | 100 | 1104 | 100 | 1104 | |
| | $T_3$ | PC ← PC + 1 | 101 | 1104 | 100 | 1104 | |
| Decode IR[15-12] | $T_4$ | MAR ← IR[11-0] | 101 | 1104 | 104 | 1104 | |
| Get operand | $T_5$ | MBR ← M[MAR] | 101 | 1104 | 104 | 0023 | |
| Execute | $T_6$ | AC ← MBR | 101 | 1104 | 104 | 0023 | 0023 |

## Revised Figure 4.14 (b) ADD 105

| Step | Step # | RTN | PC | IR | MAR | MBR | AC |
|---|---|---|---|---|---|---|---|
| (initial values AFTER LOAD 104) | | | 101 | 1104 | 104 | 0023 | 0023 |
| Fetch | $T_0$ | MAR ← PC | 101 | 1104 | 101 | 0023 | 0023 |
| | $T_1$ | MBR ← M[MAR] | 101 | 1104 | 101 | 3105 | 0023 |
| | $T_2$ | IR ← MBR | 101 | 3105 | 101 | 3105 | 0023 |
| | $T_3$ | PC ← PC + 1 | 102 | 3105 | 101 | 3105 | 0023 |
| Decode IR[15-12] | $T_4$ | MAR ← IR[11-0] | 102 | 3105 | 105 | 3105 | 0023 |
| Get operand | $T_5$ | MBR ← M[MAR] | 102 | 3105 | 105 | FFE9 | 0023 |
| Execute | $T_6$ | AC ← AC + MBR | 102 | 3105 | 105 | FFE9 | 000C |

## Revised Figure 4.14 (c) STORE 106

| Step | Step # | RTN | PC | IR | MAR | MBR | AC |
|---|---|---|---|---|---|---|---|
| (initial values AFTER LOAD 104) | | | 102 | 3105 | 105 | FFE9 | 000C |
| Fetch | $T_0$ | MAR ← PC | 102 | 3105 | 102 | FFE9 | 000C |
| | $T_1$ | MBR ← M[MAR] | 102 | 3105 | 102 | 2106 | 000C |
| | $T_2$ | IR ← MBR | 102 | 2106 | 102 | 2106 | 000C |
| | $T_3$ | PC ← PC + 1 | 103 | 2106 | 102 | 2106 | 000C |
| Decode IR[15-12] | $T_4$ | MAR ← IR[11-0] | 103 | 2106 | 106 | 2106 | 000C |
| Execute* | $T_5$ | MBR ← AC | 103 | 2106 | 106 | 000C | 000C |
| | $T_6$ | M[MAR] ← MBR | 103 | 2106 | 106 | 000C | 000C |

***** "Get Operand" step is not necessary for STORE instructions

**On page 216** of the text, the "signal patterns" for the ADD RTN seem wrong in a number of ways:

- The timing signs used are $T_0$ - $T_3$, when using $T_4$ - $T_6$ would make more sense since the "fetch" steps should be $T_0$ - $T_3$.
- "$P_0$ $P_2$ $T_1$: MBR ← M[MAR]" should be "$P_4$ $P_3$ $T_5$: MBR ← M[MAR]"
- For "AC ← AC + MBR", I'm not sure the $P_0$ and $P_1$ signals are needed since the AC and MBR are connected directly to the ALU. The $P_5$ signal makes some amount of sense if it triggers a "LOAD" of the AC.

The corrected signal patterns on page 216 should be:

$P_3$ $P_2$ $P_1$ $P_0$ $T_4$: MAR ← IR[11-0]
$P_4$ $P_3$ $T_5$: MBR ← M[MAR]
$A_0$ $P_5$ $T_6$: AC ← AC + MBR
$C_r$ $T_7$: [Reset the clock cycle counter.]