Name:_____

Homework #2 Computer Organization
Due: Febuary 13, 2009 (F)

1. Assuming each ASCII character is store as a byte (8-bits) with the most-significant bit being used for even-parity, what would the string "Computer" be as a sequence of hexadecimal values. (For example, "cab" would be: 63_{16} $E1_{16}$ $E2_{16}$)

2. The following Hamming codeword contains 8-bits of data (D_7 to D_0), and four (P_8, P_4, P_2, and P_1) even-parity bits to allow for one-bit error detection and correction. Determine if an error has occurred and correct it if possible.

12	11	10	9	8	7	6	5	4	3	2	1
D_7	D_6	D_5	D_4	P_8	D_3	D_2	D_1	P_4	D_0	P_2	P_1
0	1	1	0	0	1	0	1	1	1	1	0
4+8	1+2+8	2+8	1+8	8	1+2+4	2+4	1+4	4	1+2	2	1

3. Determine the Hamming codeword if the 8-bits of data (D_7 to D_0) are $1000\ 1101_2$, i.e., what are the values of the four even-parity bits (P_8, P_4, P_2, and P_1) to allow for one-bit error detection and correction.

12	11	10	9	8	7	6	5	4	3	2	1
D_7	D_6	D_5	D_4	P_8	D_3	D_2	D_1	P_4	D_0	P_2	P_1
4+8	1+2+8	2+8	1+8	8	1+2+4	2+4	1+4	4	1+2	2	1

4. Draw the complete circuit (i.e., no "..."s) to implement an 8-to-1 MUX (multiplexer).

5.

A	B	D	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Identity Name	AND Form	OR Form
Identity Law	$1x = x$	$0+x = x$
Null (or Dominance) Law	$0x = 0$	$1+x = 1$
Idempotent Law	$xx = x$	$x+x = x$
Inverse Law	$x\bar{x} = 0$	$x+\bar{x} = 1$
Commutative Law	$xy = yx$	$x+y = y+x$
Associative Law	$(xy)z = x(yz)$	$(x+y)+z = x+(y+z)$
Distributive Law	$x+yz = (x+y)\ (x+z)$	$x(y+z) = xy + xz$
Absorption Law	$x(x+y) = x$	$x+xy = x$
DeMorgan's Law	$\overline{(xy)} = \bar{x}+\bar{y}$	$\overline{(x+y)} = \bar{x}\bar{y}$
Double Complement Law	$\bar{\bar{x}} = x$	

For the Boolean function F represented in the above truth table:
a) write the sum-of-products (SOP) Boolean expression

b) draw the unsimplified circuit for this SOP expression. Also, determine the number of gate delays and circuit complexity (# gates + # inputs into those gates)

c) using the identities of Boolean algebra, simplify this function F as much as you can

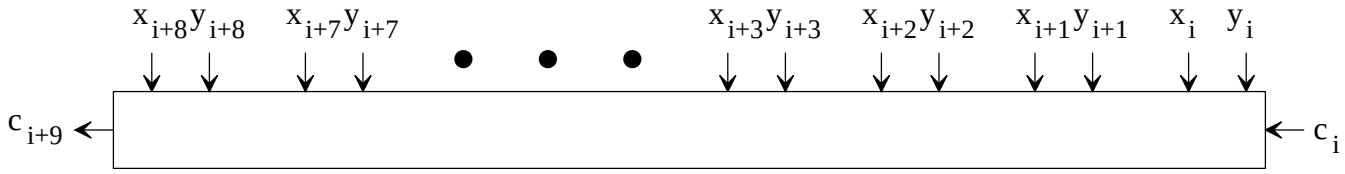
d) draw the simplified circuit for your answer in part (c). Also, determine the number of gate delays and circuit complexity (# gates + # inputs into those gates) of this circuit

6. Recall that the sum-of-products (SOP) Boolean formula for the carry-out (c_{i+1}) of a 1-bit adder was : $c_{i+1} = x_i y_i + x_i c_i + y_i c_i$.

a) Complete the following table showing the gate delays for different types of adders assuming a 9-input limit into any gate.

Type of Adder	# of product terms in SOP expression to be OR'ed	Most # of inputs in any of the product terms	# gate delays due to product/AND terms	# gate delays due to sum/OR	Gate Delay per Adder
1-bit	3	2	1	1	2
2-bit	7	3			
3-bit	15	4			
4-bit	31	5			
5-bit	63	6			
6-bit	127	7			
7-bit	255	8			
8-bit	511	9			
9-bit	1,023	10			

b) Consider the SOP Boolean formula for the carry-out (c_{i+9}) of a 9-bit adder:



Give an example of each of the following:

i) a product term with only two terms

ii) a product term with 10 terms