

## Computer Organization Spring 2009

Lect #	Tuesday		Thursday	
1	1/13	Sections 1.1 - 1.5: Intro. to Computer Organization and Computer History	1/15	Sections 2.1-2.3: Binary and Hexadecimal number systems; Unsigned Integers
3	1/20	Section 2.4: Signed Integers: two's complement	1/22	Section 2.5: IEEE 754 Floating Point: Representation, Range, Precision, and Accuracy
5	1/27	Sections 2.6-2.7: Characters; Error Correction and Detection	1/29	Sections 3.1-3.3: Boolean Algebra; Logical Gates
7	2/3	Section 3.4-3.5: Common Combinational Circuits	2/5	Section 3.6: 1-bit latches, Timing Diagrams
9	2/10	Section: 3.6: 1-bit latches, Timing Diagrams	2/12	Section: 3.6: Flip-Flops, Registers, Register File
11	2/17	Section 4.1- 4.7: CPU, Bus, Clock, I/O, Memory, Interrupts	2/19	Intro. to MARIE
13	2/24	Review for Test 1	2/26	<b>Test 1</b>
15	3/3	Section 4.8-4.10: MARIE, Fetch-decode-execute cycle, Simple MARIE AL programming	3/5	Section 4.11-4.13: MARIE assembly-language programming practice, Hardwired control unit
17	3/10	Section 4.13: MARIE Microprogrammed Control Unit	3/12	Section 4.14: Intel x86 (CISC), MIPS (RISC) architectures, MIPS assembly language introduction
<b>Spring Break: March 16 - 20</b>				
19	3/24	MIPS practice	3/26	MIPS practice and Test 2 review
21	3/31	<b>Test 2</b>	4/2	arrays, walking pointers, and run-time stack
23	4/7	MIPS calling conventions	4/9	Examples using MIPS calling conventions
25	4/14	PCSpim System calls	4/16	MIPS logical and shifting instructions
27	4/21	Usage of logical/shift instrs: bit-string set representation	4/23	Hardware Support for OS: CPU timer, privileged instructions, dual-mode CPU operation, memory protection
29	4/28	Hardware Support for OS: I/O modules and methods (programmed-I/O, interrupt-driven I/O, DMA I/O)	4/30	Hardware Support for OS: Memory-mapped vs I/O instructions; Real architectures - pipeline, superscalar, multicore systems
<b>Final:</b> Tuesday, May 5 from 8-9:50 AM in ITT 328				