Name:_____

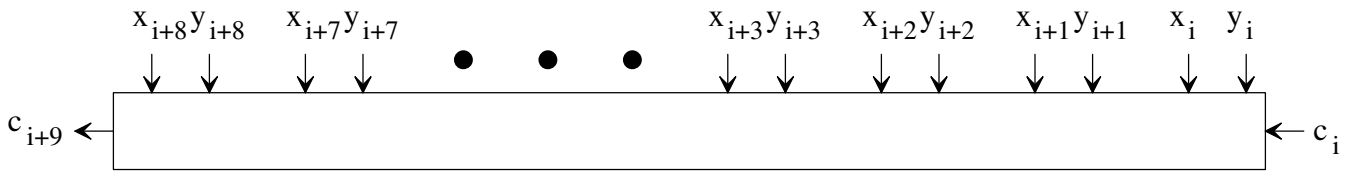
# Homework #2 Computer Organization
## Due: Febuary 11, 2011 (F)

1. Recall that the sum-of-products (SOP) Boolean formula for the carry-out ($c_{i+1}$) of a 1-bit adder was : $c_{i+1} = x_i y_i + x_i c_i + y_i c_i$.

a) Complete the following table showing the gate delays for different types of adders assuming a 9-input limit into any gate.

| Type of Adder | # of product terms in SOP expression to be OR'ed | Most # of inputs in any of the product terms | # gate delays due to product/AND terms | # gate delays due to sum/OR | Gate Delay per Adder |
|---|---|---|---|---|---|
| 1-bit | 3 | 2 | 1 | 1 | 2 |
| 2-bit | 7 | 3 | | | |
| 3-bit | 15 | 4 | | | |
| 4-bit | 31 | 5 | | | |
| 5-bit | 63 | 6 | | | |
| 6-bit | 127 | 7 | | | |
| 7-bit | 255 | 8 | | | |
| 8-bit | 511 | 9 | | | |
| 9-bit | 1,023 | 10 | | | |

b) Consider the SOP Boolean formula for the carry-out ($c_{i+9}$) of a 9-bit adder:




Give an example of each of the following:

i) a product term with only two terms

ii) a product term with 10 terms

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2) Complete the below diagram of a 4-bit register so that it is able to perform the following operations:

- parallel read/output of all bits (just look at the Q values)

Control the MUXs using the following codes:

$00_2$ - parallel write/input of all bits

$01_2$ - circular shift left one bit position (value shifted out of most-significant bit is shifted into the least-significant bit)

$10_2$ - arithmetic shift right (sign-extend the most-significant bit)

$11_2$ - logical shift right one bit position (value shifted out of least-significant bit is lost and a "0" is shifted into the most-significant bit)

Note: For each D-flip flop, the output of a MUX is used as the D-input.