Test 2 will be Thursday, April 7 in class. It will be closed book and notes, except for one 8.5” x 11” sheet of paper (front and back) with notes and the green MARIE Assembly Language handout.

**Chapter 4.**
Functionality of Computer Components: CPU, Bus, Memory, Clocks, I/O subsystems, Interrupts
CPU Basics: Fetch-Decode-Execute machine cycle, datapath including ALU and registers, control unit
Bus: types of lines (data, address, and control), types of buses (processor-memory, I/O buses), synchronous vs. asynchronous buses, bus arbitration schemes (daisy chain, centralized parallel, distributed arbitration using self-selection, distributed arbitration using collision detection)
Clocks: frequency, relationship to program performance
I/O subsystems: I/O interface, memory-mapped vs. special I/O instructions
Interrupts: causes, alters normal flow of execution, maskable vs. nonmaskable
MARIE: Architecture, Instr. Set Architecture, machine language format, RTN/RTL for instructions, Fetch-Decode-Execute cycle, I/O
Assembly Process: two-passes, symbol table, assembler directives
MARIE Hardwired Control Unit
MARIE Microprogrammed Control Unit
Tradeoffs between Hardwired vs. Microprogrammed Control Units

You should be able to translate a segment of high-level language code to MARIE assembly language.