The Final exam for Computer Organization is from 8-9:50 AM on Tuesday, May 7, in ITT 322. The test will be closed book and notes, except for **three** 8.5" x 11" sheet of paper (front and back) with notes, and your ARM Assembly Language Guide (available at: http://www.cs.uni.edu/~fienup/cs1410s13/lectures).

About 75% of the Final will focus on the material since the last test, and about 25% will focus on the material from tests 1 and 2.

Chapter 6: Performance
Moore's law and its implications
Terminology: Efficiency, Throughput, Latency, Relative Performance of Computer A to B (Speedup ratio), Benchmark, Rate
Metrics for computer performance: clock rate, MIPS (millions of instructions per second), MFLOPS (millions of floating point operations per second), CPI - (Clock cycles per instruction)
Amdahl's law

Chapter 7. Processor Control
Computer Hierarchy: levels of abstraction
Types of Control Units: hardwired vs. microprogrammed
RISC vs. CISC characteristics
Instruction pipelining, pipeline latches purpose
Pipeline stalls/delay causes:
1) structural hazards (i.e., piece of hardware needed by several stages at the same time)
2) data hazards (i.e., need a value before it is calculated) and bypass signal paths/forwarding to minimize
3) control hazards/branch delays (i.e., fetch wrong instructions before you either know it is a branch instruction or the outcome of the branch is known)
Ways to reduce the branch penalty: Branch Target Buffer
General idea of superpipelining
Superscalar processor stages:

- Instruction Fetch - obtain "next" instruction(s) from memory (I cache)
- Instruction Decode - decode instr(s) and rename user-visible registers to avoid data hazards (WAW & WAR) introduced by out-of-order execution
- Instruction *issue* - sent instruction to reservations unit associated with an appropriate execution unit (integer ALU, fl. pt. ALU, LOAD/STORE memory unit, etc.) to await execution
- Reservation station - *dispatch* instruction to execution unit when unit becomes free and all of the instruction's operand values are known
- Instruction retire - writes results of potentially out-of-order instructions back to registers to ensure correct in-order completion. Also, communicates with the reservation stages when instruction completion frees resources (e.g., "virtual" registers used in register renaming)

Chapter 9. Cache Memory and Virtual Memory Hierarchy
Memory hierarchy: levels and goals (speed, capacity, and cost)
Terminology: hit, miss, hit rate, miss rate, hit time, miss penalty; effective (avg.) memory access time
Locality of reference (temporal and spatial)
Cache types: direct mapped, fully associative, set associative; replacement algorithms
Virtual memory: pages, page frames, memory management unit (MMU), page faults, demand paging
Paging: page table, virtual to physical address translation, time and memory efficiency considerations
Page Table Organization and Page table entries (physical page #, disk page address, valid bit, dirty bit, reference bit, owner information, protection bit)
TLB (translation lookaside buffer)
Page-table Placement: searching hierarchical (two or more levels) page tables
Segmentation
Combining paging and segmentation

Hardware Support for the Operating System (sections 4.2)
You should understand the general concept of how the operating system with hardware support provide protection from user programs that:
1. go into infinite loops
2. try to access memory of other programs or the OS
3. try to access files of other programs

This involves understanding the concepts of
1. CPU timer
2. dual-mode operation of the CPU, and idea of privileged instructions and non-privileged instructions
3. ways to restrict a user program to its allocated address space

I/O sections 12.1-12.3
General I/O characteristics
I/ O Controller role and function
I/O address mapping: I/O-instructions vs. memory-mapped I/O
I/O Data Transfer: programmed I/O, interrupt-driven I/O, and direct-memory access (DMA)
General interrupt mechanism
Usage of interrupts by the hardware/operating system to restrict a user program's activities

Misc. material:
Process control blocks (PCB) and OS queues for I/O and process scheduling