Computer Organization (CS 1410) Spring 2016

Time and Place: 2:00-3:15 PM Tuesday and Thursday in ITT 328

eLearning Site: CS 1410 Computer Organization Section 01 Spring 2016
Course website: www.cs.uni.edu/~fienup/cs1410s16/

Class Email List: Send messages to CS-1410-01-SPRING@uni.edu from your UNI account

Instructor: Mark Fienup (fienup@cs.uni.edu)
Office: ITTC 313
Phone: 273-5918 (Home 266-5379)
Office Hours: M: 8-11:45, 1:10-3, T: 9:30-10:45, 1:10-3, W: 1:10-3, Th: 9:30-10:45, 1:10-3, F: 8-11:45

Pre- or Co-requisite: Intro. to Computing (CS 1510) or any programming course

Goals: After this course, you should understand: (1) how data is represented and manipulated on the computer, (2) simple combinational and memory circuits used to build computer components, (3) how these circuits are organized to build a computer, (4) how to program in assembly language, (5) how high-level language programming languages are implemented with respect to the run-time stack and built-in data structures such as arrays and records, and (5) general concepts of hardware support necessary for an operating system.

Required Text: *Essentials of Computer Organization and Architecture*, 4th edition, by Linda Null and Julia Lobur. Jones and Bartlett Learning, 2015. ISBN-13: 978-1-284-04561-1.

Assignments: Assignments will be both "pencil-and-paper" exercises and assembly-language programming.

Pedagogic Approach: This is a "*flipped*" class! Before coming to each class, you will be asked to do the assigned reading, watch mini-lecture video(s), and take eLearning quiz(zes). The pre-class activities frees up class time to focus on the more challenging content of the course. In class, we'll dive into active and group learning worksheets and activities. As necessary I'll do mini-lectures with a group of students or the whole class if extra explanation is needed. While the in-class worksheets (etc.) are not formally graded, part (5%) of your grade will be based on your participation in these in-class activities.

Grading policy: There will be three tests (including the final). I'll announce tests at least one week in advance to allow you time to prepare. Tentative weighting of course components is:

Pre-class Work:	15%
In-class Work:	5 %
Assignments:	20 %
In-class Test 1:	20 % (February 18)
In-class Test 2:	20 % (March 31)
Final:	20 % (Thursday, May 5 from 10 - 11:50 AM in ITT 328)

Grades will be assigned based on straight percentages off the top student score. If the top student's score is 92%, then the grading scale will be, i.e., 100-82 A, 81.9-72 B, 71.9-62 C, 61.9-52 D, and below 52 F. Plus and minus grades will be assigned for students near cutoff points.

Scholastic Conduct: You are responsible for being familiar with the University' Academic Ethics Policies (http://www.uni.edu/pres/policies/301.shtml). Copying from other students is expressly forbidden. Doing so on exams or assignments will be penalized every time it is discovered. The penalty can vary from zero credit for the copied items (first offense) up to a failing grade for the course. If an assignment makes you realize you don't understand the material, ask questions designed to improve your understanding, *not* ones designed to discover how another student solved the assignment. The solutions to assignments should be **individual, original** work unless otherwise specified. Remember: discussing assignments is good. Copying code or test-question answers is cheating.

Any substantive contribution to your assignment solution by another person or taken from a publication (**or the**

web) should be properly acknowledged in writing. Failure to do so is plagiarism and will necessitate disciplinary action. In addition to the activities we can all agree are cheating (plagiarism, bringing notes to a closed book exam, etc), assisting or collaborating on cheating is cheating. Cheating can result in failing the course and/or more severe disciplinary actions.

Special Notices:

- In compliance with the University of Northern Iowa policy and equal access laws, I am available to discuss appropriate academic accommodations that may be required for students with disabilities.
  Requests for academic accommodations are to be made during the first three weeks of the semester, except for unusual circumstances, so arrangements can be made. Students are encouraged to register with Student Disability Services, 103 Student Health Center, to verify their eligibility for appropriate accommodations.

- I encourage you to utilize the Academic Learning Center's free assistance with writing, math, science, reading, and learning strategies. UNI's Academic Learning Center is located in 008 ITTC. Visit the website at http://www.uni.edu/unialc/ or phone 319-273-2361 for more information.

Computer Organization Spring 2016

Lect #	Tuesday		Thursday	
1	1/12	Sect 1.1-1.8: Introduction, Terminology, and Computer History	1/14	Sect 2.1-2.3: Unsigned integer numbers; Converting between base 10, 2, and 16
3	1/19	Sect 2.4: Signed integers	1/21	Sect 2.5: Floating Point Representation
5	1/26	Sect 2.6-2.7: Character representation and Error Detection and Correction	1/28	Sect 3.1-3.3: Boolean logic and Gates
7	2/2	Sect 3.4-3.5: Digital Components: decoders, multiplexers, adders	2/4	Sect 3.6: 1-bit memories: SR-latch, timing diagrams, D-latch, D-flip flop, Shift register & Register file
9	2/9	Register file vs. Square-Memory RAM	2/11	Sect 4.8: MARIE architecture and assembly language
11	2/16	Review for Test 1	2/18	**Test 1**
13	2/23	4.1-4.9: MARIE CPU, Bus, Clock, I/O, Memory, and RTL/RTN	2/25	Sect 4.10-4.13: MARIE Hardwired Control Unit
15	3/1	MARIE Microprogrammed Control Unit	3/3	Sect 4.14: MIPS Architecture and Assembly Language Control structures
17	3/8	Sect 4.14: MIPS Assembly Language 1D-Array Examples	3/10	Practice MIPS; Walking pointers in an array and 2-D arrays
Spring Break				
19	3/22	Run-time stack in HLL; CalculatePowers MIPS calling convention example	3/24	Insertion Sort MIPS calling convention example
21	3/29	Review for Test 2	3/31	**Test 2**
23	4/5	PCSpim I/O; MIPS Logical and shift instruction	4/7	Sect 8.1-8.2: Hardware support for OS: CPU timer, privileged instrs, dual-mode CPU, memory protection; Sect 7.1-7.4: I/O modules and methods (programmed-I/O, interrupt-driven I/O, DMA I/O) Sect 9.1-9.4: Memory-mapped vs. I/O instructions
25	4/12	Sect 8.1-8.2: OS queues and process mgt; Instr Pipelining; Data and control hazards	4/14	Dynamic Branch Prediction: Branch-Prediction Buffer (BPB/BHT)
27	4/19	Superscalar, WAR & WAW dependencies; Ch 5: Memory Hierarchy and cache	4/21	Virtual Memory: paging, page table, TLB, segmentation and combining
29	4/26	Virtual Memory Examples	4/28	Review for Final
Final: Thursday, May 5 from 10:00 to 11:50 AM in ITT 328				