Name:_____

Homework #2 Computer Organization
Due: Feb 8, 2019 (Friday) by 3 PM

1. Assuming each ASCII character is store as a byte (8-bits) **WITH THE MOST-SIGNIFICANT BIT BEING USED FOR EVEN-PARITY**. What would the string "Fienup" be as a sequence of hexadecimal values. (For example, "cab" would be: 63_{16} $E1_{16}$ $E2_{16}$)

2. The following Hamming codeword contains 8-bits of data (D_7 to D_0), and four (P_8, P_4, P_2, and P_1) even-parity bits to allow for one-bit error detection and correction. Determine if an error has occurred and correct it if possible.

12	11	10	9	8	7	6	5	4	3	2	1
D_7	D_6	D_5	D_4	P_8	D_3	D_2	D_1	P_4	D_0	P_2	P_1
1	1	0	1	1	1	0	1	0	1	1	0
4+8	1+2+8	2+8	1+8	8	1+2+4	2+4	1+4	4	1+2	2	1

3. Determine the Hamming codeword if the 8-bits of data (D_7 to D_0) are $0101\ 1101_2$, i.e., what are the values of the four even-parity bits (P_8, P_4, P_2, and P_1) to allow for one-bit error detection and correction.

12	11	10	9	8	7	6	5	4	3	2	1
D_7	D_6	D_5	D_4	P_8	D_3	D_2	D_1	P_4	D_0	P_2	P_1
4+8	1+2+8	2+8	1+8	8	1+2+4	2+4	1+4	4	1+2	2	1

4. Let $D = 1011001010111010_2$ (16-bit data) with $G = x^5 + x^2 + 1$ is 100101_2 (degree 5 polynomial)

a) Determine the CRC remainder:

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1 0 0 1 0 1 ) 1 0 1 1 0 0 1 0 1 0 1 1 1 0 1 0 0 0 0 0 0
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append 5 0's since G has 6 bits, so the remainder will have 5 bits

b) Determine the codeword sent which is the data appended with the (5-bit) remainder.

c) Divide the codeword by the generator $G = x^5 + x^2 + 1$ (100101_2) to check for an error. Remainder should be zero if no errors.

d) Introduce some random error into the codeword and check for an error by dividing by the generator $G = x^5 + x^2 + 1$ (100101_2)

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5.

A	B	C	D	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

Identity Name	AND Form	OR Form
Identity Law	$1x=x$	$0+x=x$
Null (or Dominance) Law	$0x=0$	$1+x=1$
Idempotent Law	$xx=x$	$x+x=x$
Inverse Law	$x\bar{x}=0$	$x+\bar{x}=1$
Commutative Law	$xy=yx$	$x+y=y+x$
Associative Law	$(xy)z=x(yz)$	$(x+y)+z=x+(y+z)$
Distributive Law	$x+yz=(x+y)\,(x+z)$	$x(y+z)=xy+xz$
Absorption Law	$x(x+y)=x$	$x+xy=x$
DeMorgan's Law	$(\overline{xy})=\bar{x}+\bar{y}$	$(\overline{x+y})=\bar{x}\bar{y}$
Double Complement Law	$\bar{\bar{x}}=x$	

For the Boolean function F represented in the truth table:

a) write the sum-of-products (SOP) Boolean expression (i.e., where are the 1's are in the F column, F = $\bar{A}\bar{B}\bar{C}\bar{D}+\bar{A}\bar{B}\bar{C}D+...$

b) draw the unsimplified circuit for this SOP expression, **and** determine the number of gate delays and circuit complexity (# gates + # inputs into those gates)

c) using a K-map (or the identities of Boolean algebra) , simplify this function F as much as you can

d) draw the simplified circuit for your answer in part (c), **and** determine the number of gate delays and circuit complexity (# gates + # inputs into those gates) of this circuit

6. Draw the circuit (using AND, OR, and NOT gates) to implement a 32-input to 1-output multiplexer (MUX). Your MUX should have 5 control wires (c_4, c_3, c_2, c_1, c_0) to select which input is switched to the single output. (You can use ". . ." to avoid drawing all the AND-gates of the whole MUX, but show enough to demonstrate your understanding of MUXs). Assume there is a 9-input limit to AND and OR gates.

b) How many gate delays does your MUX have?