1. How does a hierarchy of buses instead of a single Memory-I/O bus improve performance of a computer system?

2. What is the purpose of the “Bridge”s in a bus hierarchy?

3. In the PCI Read figure, why is a turn-around cycle needed between sending of the Address and Data on the AD lines?

4. (see next page)

5. In the PCI protocol each device has its own set of dedicated bus arbitration lines. All of the arbitration lines go to a centralized arbitrator. Why does the PCI protocol not specify a specific arbitration scheme (such as first-come-first-serve)?
4. Draw and explain a timing diagram for a PCI read operation (similar to Figure 3.23). Assume that 2 data transfers occur and that the following occurs during these transfers:
- during the first data transfer the initiator is not ready for two clock cycles, and
- during the second data transfer the target is not ready for one clock cycle.

On your diagram clearly indicate:
- the address phase, data phase(s) and any wait states
- which wire(s) are controlled by the target device and which are controlled by the initiator device
- when the “target” reads the data off the bus