

The final will be 10-11:50 AM on Thursday, December 13 in ITT 322. The test will be closed-book and closed-note, except for three sheets of paper with notes. About 70% of the Final will focus on the material since the last test, and about 30% will focus on tests 1 and 2 material.

### **Chapter 9.1-9.4.1 Alternate Architectures (and lecture 21 notes:**

<http://cns2.uni.edu/~fienu/cs142f07/lectures/lec21.pdf>)

RISC machines: RISC vs. CISC, overlapping register windows

Flynn's taxonomy

Superpipelining

Superscalar characteristics

Instruction-level parallelism and its limitations due to write-read/RAW data dependencies, procedural dependencies, and resource conflicts.

Machine-level parallelism

Instruction-issue policies: In-order Issue with In-order Completion, In-order Issue with Out-of-Order Completion, and Out-of-Order Issue with Out-of-Order Completion

Dependencies: true data dependencies (read-after-write/RAW), output (write-write/WAW) dependencies, antidependencies (read-write/WAR)

Instruction window, Register renaming, Tomasulo's algorithm

General understanding of the Pentium 4 pipeline (DON'T memory stages, but just try to get the general concepts)

IA-64 / Itanium Features:

- \* Uses *explicit parallel instruction computing (EPIC)* from *very-long-instruction-word (VLIW)* architecture.

- \* Provides hardware support for efficient procedure calls and returns via large number of registers with overlapping register windows

- \* Branch predication (NOT branch prediction) that allows speculative execution along both paths of a branch

### **Multiprocessor Systems (Power Point Presentations) and Chapter 9**

#### **Introduction to Multiprocessors**

Need for multiprocessors and clusters

Amdahl's law

Trends in supercomputers (Top 500) toward clusters

Flynn's Classification: SISD, SIMD, MISD, MIMD

Multiprocessor basic organizations: Communication models (message passing vs. shared memory(UMA, NUMA) and physical connection (network vs. bus)

#### **Bus Connected Multiprocessors**

Single bus multiprocessor issues: cache coherency, process synchronization, spin locks

#### **Network Connected Multiprocessors**

Network connected multiprocessors: message passing (sends & receives), cache coherency in NUMAs (directory-base protocols)

Interconnection network (IN) metrics: cost (# switches, links/switch, link width, link length), network bandwidth, bisection bandwidth, others (latency, throughput, # routing hops)

Interconnection network types: bus, ring, fully connected, crossbar, hypercube, 2D & 3D mesh/torus, fat tree  
Network of Workstations (NOW) Clusters

#### **Multicore processors**

Performance issues related to the memory hierarchy, e.g., the need for data reuses

Current Multicore Problems: small caches, TLB not covering caches, memory bandwidth bottleneck

Motivation of multithreading on a chip: hide stalls due to dependency, cache misses, etc. and thus increase utilization of functional units

Types of multithreading on a chip: fine-grain, coarse-grain, simultaneous multithreading (SMT)