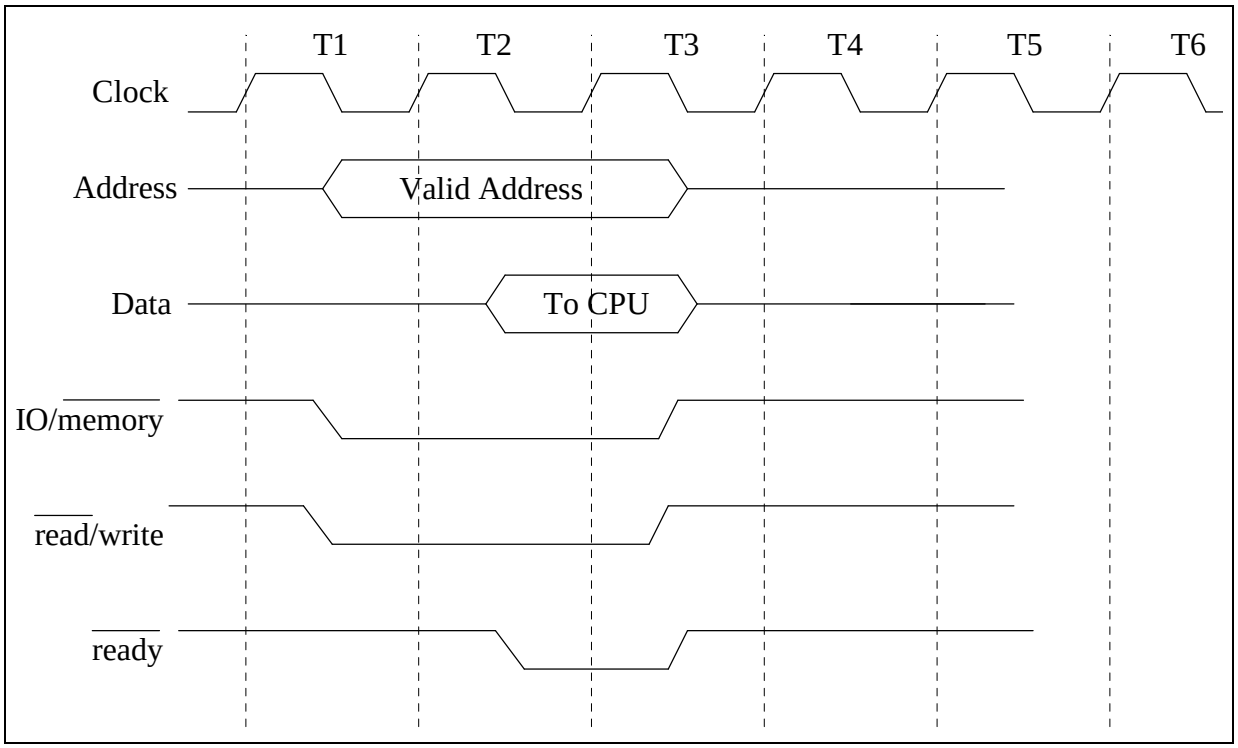
Name:_____ 10/18/07

Synchronous Bus

Synchronous Bus - Actions happen relation to the clock cycle, e.g., devices write things to the bus in the middle of a clock cycle and read the bus on the clock cycle.

Memory read operation with no wait states.



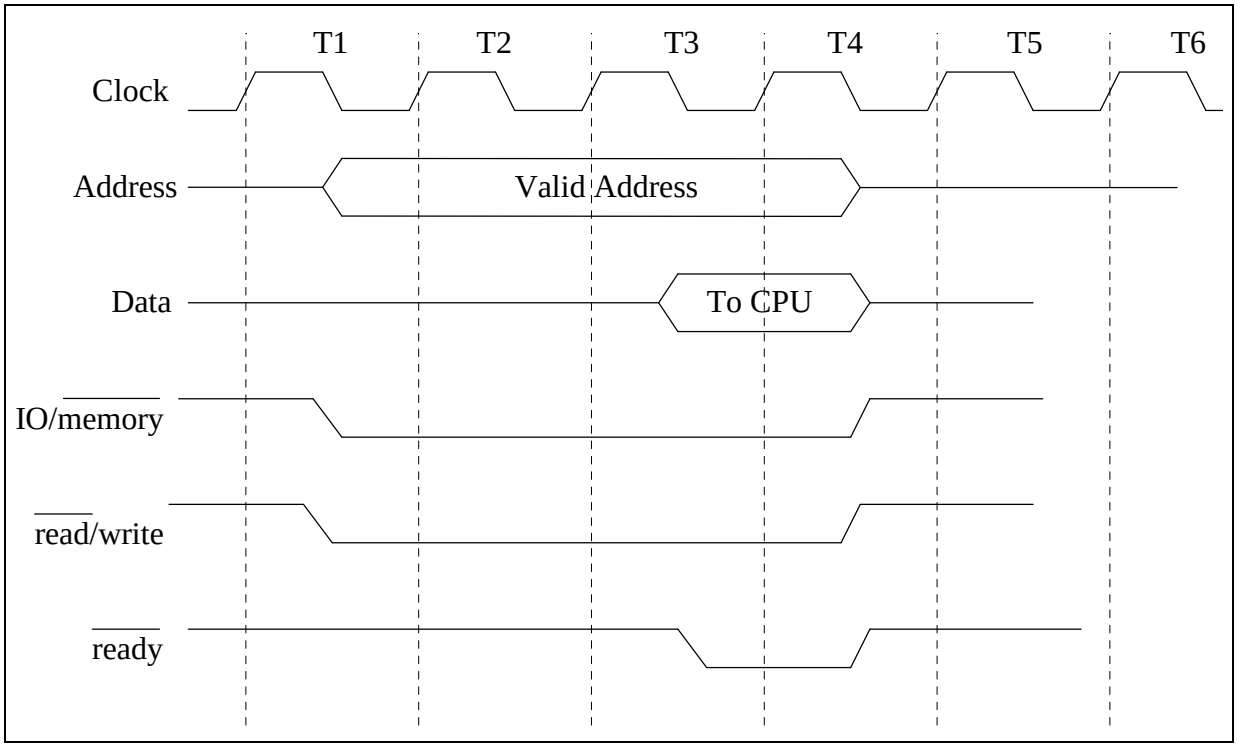
CPU puts Address on command (memory read) on bus in middle of clock cycle T1

Memory looks at the bus at the start of T2 and sees the address and command. We assume here that the memory can supply the data "immediately", and puts the Data and the *ready* signal (indicates that the data is available on the Data lines).

CPU looks at the bus at the start of T3 and sees that the data is available because the *ready* signal is asserted. The CPU removes the address, IO/memory, and read/write signals.

Name:_____ 10/18/07

Memory read operation with one wait states.



CPU puts Address on command (memory read) on bus in middle of clock cycle T1

Memory looks at the bus at the start of T2 and sees the address and command. We assume here that the memory **cannot** supply the data "immediately", and must wait one cycle to put the Data and the $\overline{ready}$ signal on the bus.

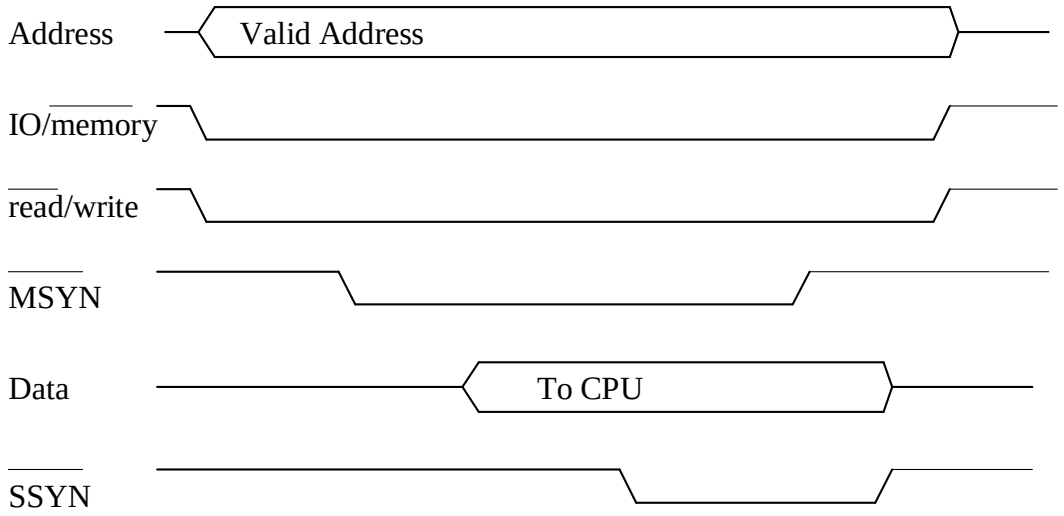
CPU looks at the bus at the start of T4 and sees that the data is available because the $\overline{ready}$ signal is asserted. The CPU removes the address, IO/memory, and read/write signals.

Name:_____ 10/18/07

Asynchronous Bus

Handshaking is used to control the bus transaction.

Memory read operation.



1) Bus Master/CPU - puts Address and command (memory read) on the bus
2) After the CPU is certain the signals have reached the “slave”/memory, it asserts MSYN
3) Memory work and puts the Data on the bus
4) After the memory is certain the signals have reached the “master”/CPU, it asserts the SSYN
5) CPU reads the Data and deasserts MSYN to indicate that the data has been received
6) On seeing the MSYN deasserted, the Memory knows it can quit sending the data and SSYN

Name:_____ 10/18/07

a) In the above asynchronous READ timing diagram shown, how does the Master know that the data is available on the Data lines?

b) In the asynchronous READ timing diagram shown, how is bus skew handed?