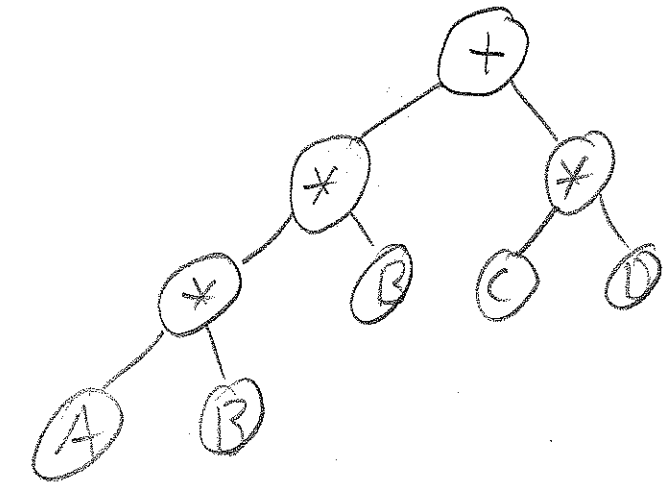
# Comp. Arch. HW #1

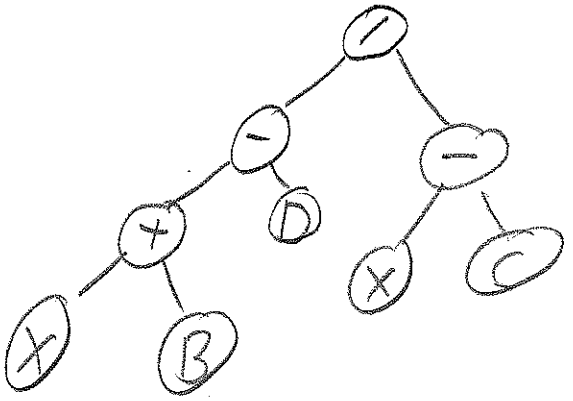
$$X = A * B * B + C * D$$

$$Y = (X + B - D) / (X - C)$$




Postorder:

A B * B * C D * +




X B + D - X C - /

## 3 Address

```
MUL X,A,B
MUL X,X,B
MUL T,C,D
ADD X,X,T
```

```
ADD T,X,B
SUB T,T,D
SUB T2,X,C
DIV Y,T,T2
```

Instruction Fetches: $8 \times (8+32+32+32) = 8 \times 104 = 832$ bits

Data $8 \times 3 \times 32 = 768$ bits

Total = $832 + 768 = 1600$ bits

## 2-Address

```
MOVE X, A
MUL X, B
MUL X, B
MOVE T, C
MUL T, D
ADD X, T
MOVE Y, X
ADD Y, B
SUB Y, D
MOVE T, X
SUB T, C
DIV Y, T
```

Fetch Instrs = 12 × (8+32+32)
= 12 × 72 = 864 bits

Data transfers:
MOVES 4 × (32+32) = 256
Other: 8 × (32+32+32) = 768
1024 bits

Total bits = 1888 bits

## 1-Address

```
LOAD A
MUL B
MUL B
STORE X
LOAD C
MUL D
ADD X
STORE X
SUB C
STORE T
LOAD X
ADD B
SUB D
DIV T
STORE Y
```

Fetch Instrs = 15 × (8+32)
= 600 bits

Data transfers = 15 × 32
= 480 bits

Total bits = 1080 bits

## 0-Address

```
PUSH A
PUSH B
MUL
PUSH B
MUL
PUSH C
PUSH D
MUL
ADD
POP X
PUSH X
PUSH B
ADD
PUSH D
SUB
PUSH X
PUSH C
SUB
DIV
POP Y
```

Instr Fetches: $12 \times (8+32) + 8 \times 8$
$= 480 + 64 = 544$ bits

DATA $= 12 \times 32 = 384$ bits

Total = 928 bits

## Load/Store

```
LOAD  R1, A
LOAD  R2, B
MUL   R3, R1, R2
MUL   R3, R3, R2
LOAD  R4, C
LOAD  R5, D
MUL   R6, R4, R5
ADD   R3, R3, R6
STORE R3, X
ADD   R7, R3, R2
SUB   R7, R7, R5
SUB   R8, R3, R4
DIV   R7, R7, R8
STORE R7, Y
```

Instr Fetches:

$6 \times (8+5+32) = 270$

$8 \times (8+5+5+5) = 184$

454 bits

Data:

$6 \times 32 = 192$ bits

Total = 646 bits