Computer Architecture HW #5

Due: Friday, Oct. 16 (5 PM in ITT 305 mailbox or under my door, ITT 313)

1. Draw the timing diagrams of Figure 3.20 including arrows showing cause-and-effect relationships and delays for bus skew.

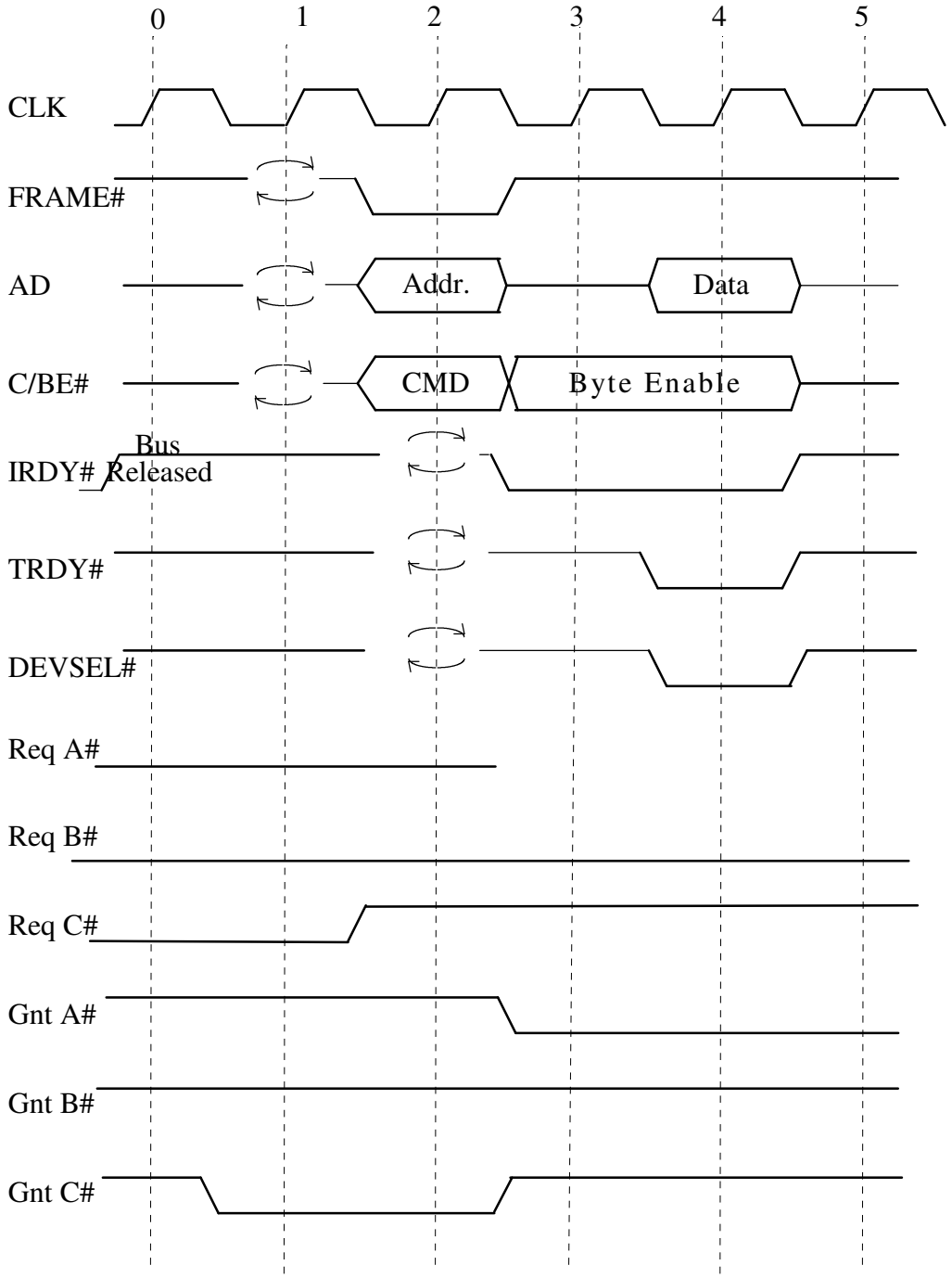
2. Draw and explain a timing diagram for a PCI write operation. Assume that 3 data transfers occur and that the following occurs during these transfers:
   - during the first data transfer the target is not ready for three clock cycles,
   - during the second data transfer the initiator is not ready for one clock cycle, and
   - during the third data transfer, the target is not ready for two clock cycles.

You are to draw a diagram similar to Figure 3.23. On your diagram clearly indicate:
   - the address and data phases and any wait states,
   - which wire(s) are controlled by the target device, initiator device, or both, and
   - when the data is read off the bus by the target.

3. Complete the below timing diagram for the following sequence of bus transactions:
   - device A wants to do a write transfer and has asserted REQ A# at the start of cycle 0
   - device B wants to do a write transfer and has asserted REQ B# at the start of cycle 0
   - device C wants to do a read transfer and has asserted REQ C# at the start of cycle 0

Make the following assumptions:
   - devices A, B, and C all only want to transfer one piece of datum
   - the arbiter uses a round-robin priority scheme where currently Device C has the highest priority and device Device B has the lowest priority
   - for all three data transfers, both the initiator and target are ready as soon as possible
   - Before cycle 0 starts, the previous bus users deassert FRAME# and DEVSEL# so it is free

The below figure shows the request (REQ#) and grant (GNT#) lines. Notice the hidden arbitration that PCI uses to hide arbitration.


0
1
2
3
4
5
CLK
FRAME#
AD
Addr.
Data
C/BE#
CMD
Byte Enable
IRDY#
Bus Released
TRDY#
DEVSEL#
Req A#
Req B#
Req C#
Gnt A#
Gnt B#
Gnt C#