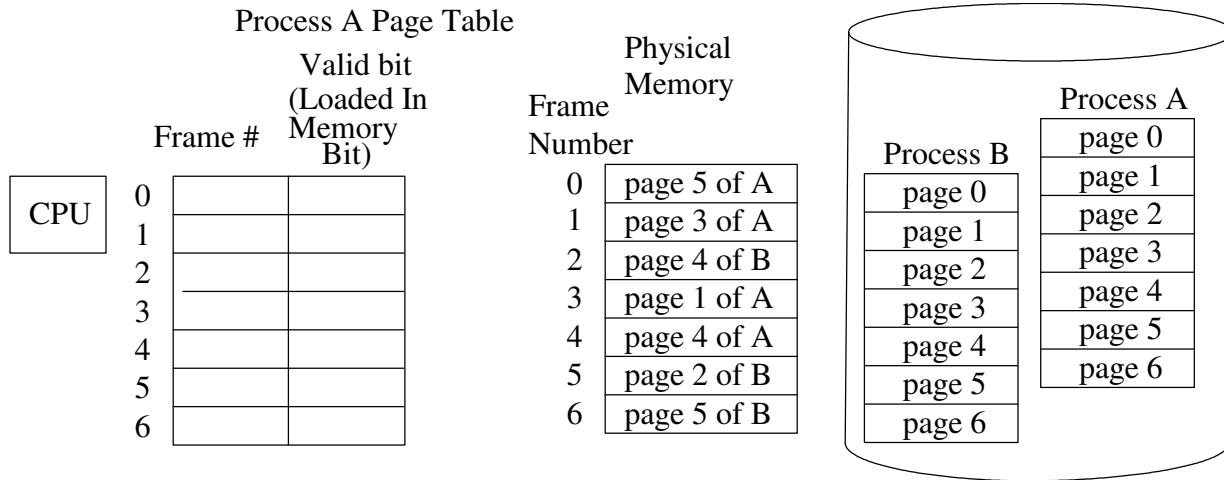


# Computer Architecture Homework #8

## Due: December 4, 2009 (Friday 5 PM)

Chapter 8. Exercises: 8.6, 8.14, and 8.17 (copies to this problems can be found at [http://www.cs.uni.edu/~fienup/cs142f09/homework/hw8\\_ch8\\_exercises.pdf](http://www.cs.uni.edu/~fienup/cs142f09/homework/hw8_ch8_exercises.pdf)) and the following problems:

1. Consider the demand paging system with 1024-byte pages.



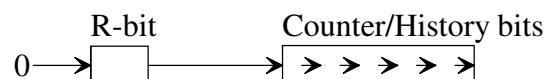
a) Complete the above page table for **Process A**.

b) If process A is currently running and the CPU generates a logical/virtual address of  $3108_{10}$ , then what would be the corresponding physical address?

2. For a paged memory system with a TLB (translation-lookaside buffer) and a L1 cache, what steps would be in the fastest memory access assuming that the L1 cache is **tagged with physical memory addresses**?

3. For a paged memory system with a TLB (translation-lookaside buffer) and a L1 cache, what steps would be in the fastest memory access assuming that the L1 cache is **tagged with virtual addresses**?

4. To approximate the LRU page-replacement algorithm most hardware supports the updating/setting of a reference bit (R-bit) in the page-table entry corresponding to each memory reference. To get a better approximation of LRU, additional counter/history bits can be maintained. Periodically, say every 10 milliseconds, the process is interrupted so the OS can shift the R-bit into the counter/history bits for each page-table entry and clear the R-bits. Such as

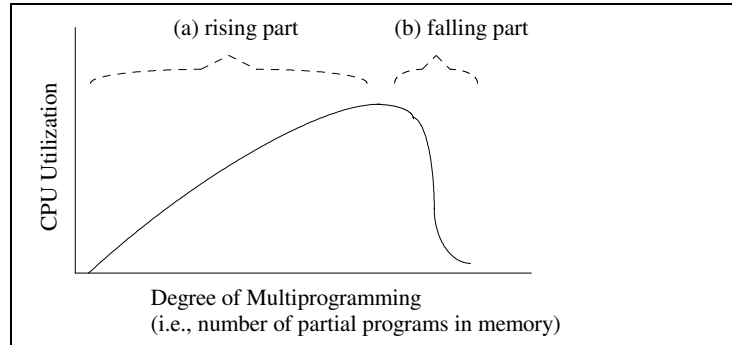


a) If the pages in main memory have the below R-bit and counter/history bits, then which page should be selected for replacement on a page fault?

Page	R-bit	Counter/History bits
0	1	0 0 0 1 0 1 0
1	0	0 0 0 0 1 1 0
2	0	0 0 1 0 0 0 0
3	0	0 0 1 1 0 1 0
4	1	1 0 0 0 0 1 0

b) If the R-bits are shifted every 10 milliseconds and R-bits are about to be shifted because the interrupt just occurred, how long (specify a range) has it been since page 3 was referenced?

5. Consider the following performance curve that is expected for a paged memory system.



Explain the shape of each section indicated on the above curve:

a) (rising part of the curve)

b) (falling part of the curve)

c) What should the operating system do if it detects that thrashing (the falling part of the curve) is occurring?

6. Consider the combination of paging with segmentation by paging each segment as shown in the following diagram. Assume that the page size is 1024 bytes.

a) If process X is currently running and the CPU generates a logical/virtual address of <Segment 1, Segment offset of  $14_{10}$ >, then what would be the corresponding physical address?

b) Complete the page table for Process X **Segment 4**.

