1) In Figure 3.19 (synchronous read), how was bus skew handled?

2) In Figure 3.20 (a) where the CPU is reading from Memory, which device is driving the wires:
   a) Status lines?
   b) Address lines?
   c) Read?
   d) Data lines?
   e) Acknowledge?

3) In Figure 3.20(a) (asynchronous read), how was bus skew handled?

4) In the PCI protocol each device has its own set of dedicated bus arbitration lines. All of
   the arbitration lines go to a centralized arbitrator. Why does the PCI protocol not specify a
   specific arbitration scheme (such as first-come-first-serve)?

5) (on next page)

6) How does a hierarchy of buses as shown in Figure 3.22 improve performance of a computer
   system?

7) What is the purpose of the “Bridge”s as shown in Figure 3.22?
5) Draw and explain a timing diagram for a PCI read operation (similar to Figure 3.23). Assume that 2 data transfers occur and that the following occurs during these transfers:

- during the first data transfer the initiator is not ready for two clock cycles, and
- during the second data transfer the target is not ready for one clock cycle.

On your diagram clearly indicate:

- the address phase, data phase(s) and any wait states
- which wire(s) are controlled by the target device and which are controlled by the initiator device
- when the “target” reads the data off the bus