

1 Square-memory implementations of large memories often support fast page-modes that allow a burst of consecutive memory reads from within the same row of the square memory.

a) How does this benefit performance on a cache miss?

b) An additional improvement allows the processor to specify a different ordering of the consecutive memory reads. For example, a processor might specify a burst of size 4 reads with offsets of 2-3-0-1 from the specified memory address. How does this benefit performance on a cache miss?

2 a) For the 8-bit data  $01001011_2$  develop the Hamming codeword for one-bit error detection and correction:

12	11	10	9	8	7	6	5	4	3	2	1
$D_7$	$D_6$	$D_5$	$D_4$	$C_8$	$D_3$	$D_2$	$D_1$	$C_4$	$D_0$	$C_2$	$C_1$
0	1	0	0		1	0	1		1		
4+8	1+2+8	2+8	1+8	8	1+2+4	2+4	1+4	4	1+2	2	1

Check bit  $C_1$  looks at bit positions 3, 5, 7, 9, and 11

Check bit  $C_2$  looks at bit positions 3, 6, 7, 10, and 11

Check bit  $C_4$  looks at bit positions 5, 6, 7, and 12

Check bit  $C_8$  looks at bit positions 9, 10, 11, and 12

b) If bit  $D_5$  gets flipped (an error), then how would we be able to detect an error?

c) If bit  $D_5$  gets flipped (an error), then how would we be able to know which bit to correct?

d) For the 8-bit data  $11001001_2$  develop the Hamming codeword for one-bit error detection and correction:

12	11	10	9	8	7	6	5	4	3	2	1
$D_7$	$D_6$	$D_5$	$D_4$	$C_8$	$D_3$	$D_2$	$D_1$	$C_4$	$D_0$	$C_2$	$C_1$
0	1	0	0		1	0	1		1		
4+8	1+2+8	2+8	1+8	8	1+2+4	2+4	1+4	4	1+2	2	1