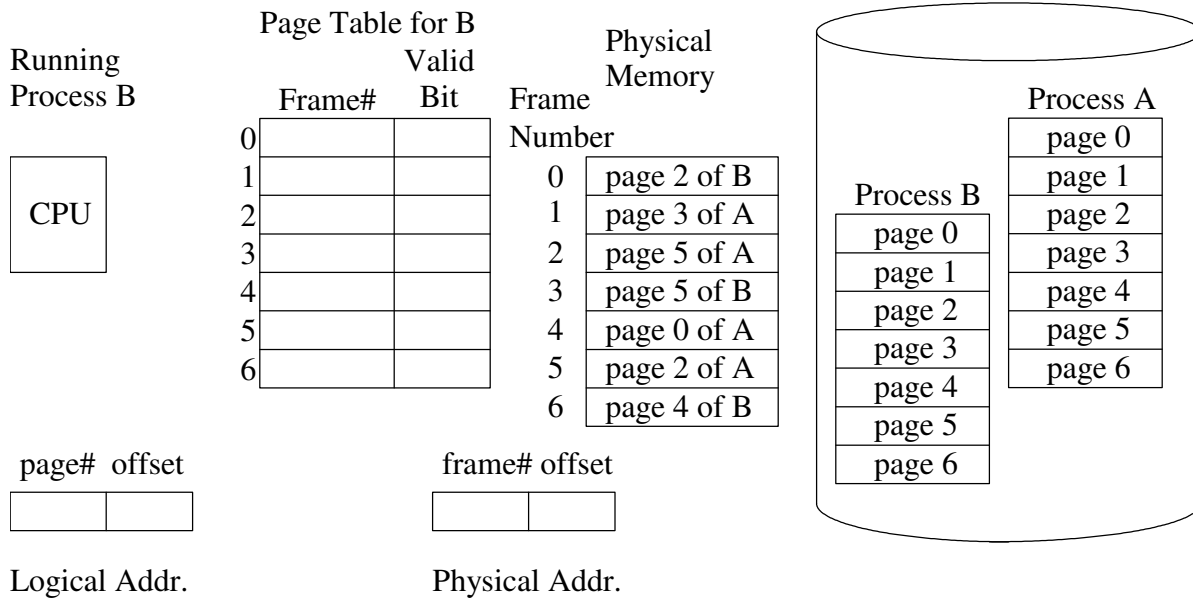


1. Consider the demand paging system with 1024-byte pages.



a) Complete the above page table for **Process B**.

b) If process B is currently running and the CPU generates a logical/virtual address of 2060_{10} , then what would be the corresponding physical address?

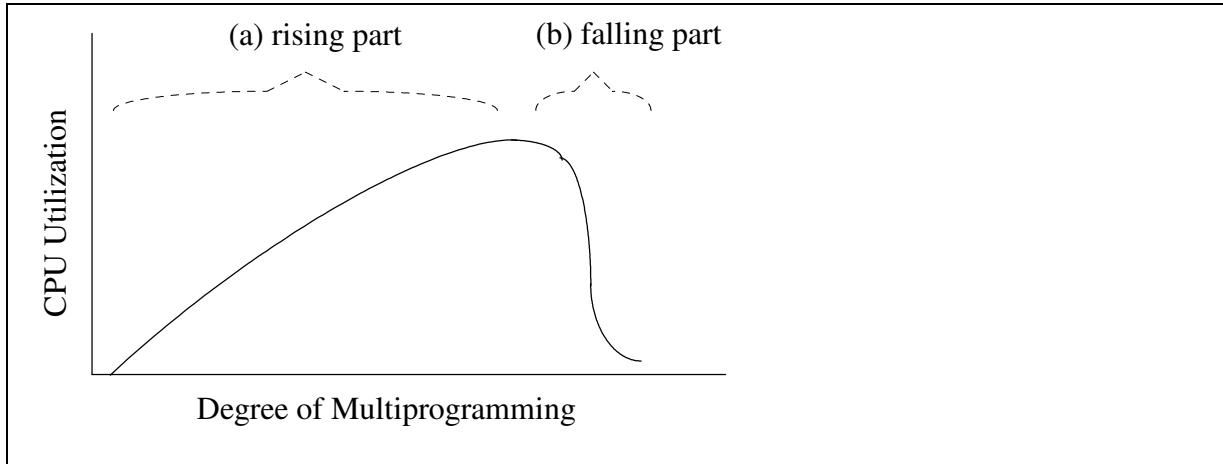
2. How does a TLB (translation-lookaside buffer) speed the process of address translation?

3. Blocks in the L1 cache can be tagged with physical/actual memory addresses, or by virtual addresses. What would be the advantage of having blocks in the L1 cache be tagged with virtual addresses?

Design issues for Paging Systems

Conflicting Goals:

- Want as many (partial) processes in memory (high degree of multiprogramming) as possible so we have better CPU & I/O utilization \Rightarrow allocate as few page frames as possible to each process
- Want as low of page-fault rate as possible \Rightarrow allocate enough page frames to hold all of a process' current working set (which is dynamic as a process changes locality)



4. Explain the shape of each section indicated on the above curve:

a) (rising part of the curve)

b) (falling part of the curve)

5. Complete the following table assuming a FIFO page-replacement algorithm and four page frames allocated to the process.

References String:	1	2	3	4	1	2	5	1	2	3	4	5
Page Frames Allocated = 4												

Number of page faults?

Page-fault rate?