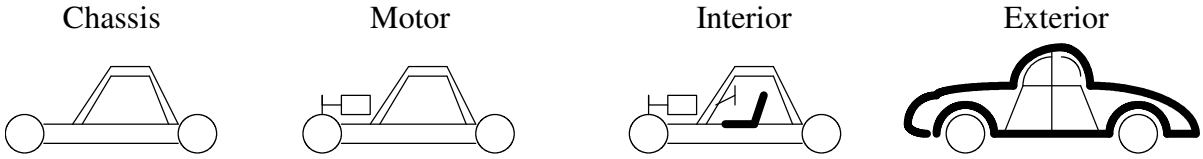
Name:_____

1. Assume that an automobile assembly process takes 4 hours.



If the stages take the following amounts of time, then what is the time between completions of automobiles?
Chassis 45 minutes
Motor 1 hour
Interior 1 hour and 15 minutes
Exterior 1 hour

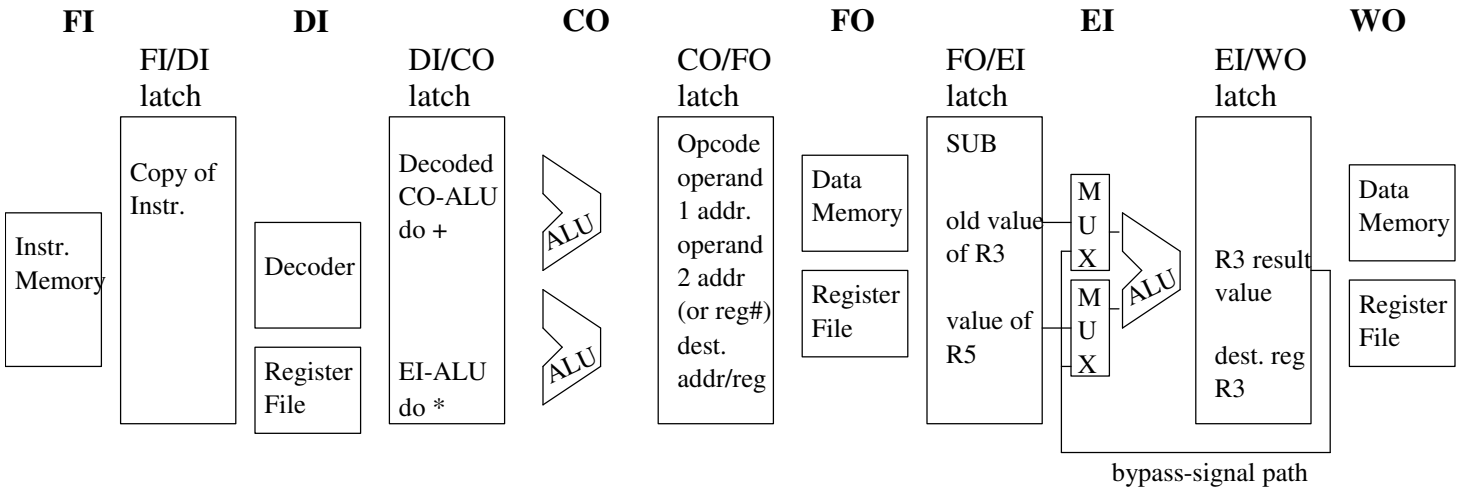
2. Consider the 6 stage (FI, DI, CO, FO, EI, WO) instruction pipelining discussed and the following assembly language segment:

```
ADD  R3, R2, R1      ; R3← R2 + R1
SUB  R4, R3, R5      ; R4 ← R3 + R5
```

a) In what stage does the ADD instruction update R3?

b) In what stage does the SUB instruction read R3?

c) In what stage does the SUB instruction execute with the R3 value?



3. What would control the MUXs of the above bypass-signal path?

Name:_____

4. Consider the following code: ADD R3, R2, R1
LOAD R4, 4(R3)

What would the timing be **without** bypass-signal paths/forwarding (use "stalls" to solve the data hazard)?

	Time →														
Instructions	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
ADD R3, R2, R1	FI	DI	CO	FO	EI	WO									
LOAD R4, 4(R3)		FI													

(Assume that R3 cannot be written and the new value read in the same stage.)

5. What would the timing be **with** bypass-signal paths?

	Time →														
Instructions	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
ADD R3, R2, R1	FI	DI	CO	FO	EI	WO									
LOAD R4, 4(R3)		FI													

6. Draw the bypass-signal paths needed for the above example.