

Test 1 for Computer Architecture will be Thursday, Oct. 1 in class. The test will be closed book and notes, except for a single page of notes (8.5" x 11" front and back). Test 1 review topics are:

Chapter 2. (Sections 2.1 - 2.3 mostly)

History of the Computer: First Generation to later generations

Utilizing processor speed: branch prediction, data flow analysis, speculative execution

Performance balance: processor, memory, I/O devices, interconnection structure

Improvements in chip organization and architecture

Evolution of Intel x86 architecture

Chapter 10 and 11 and background:

High-level programming view: Run-time stack, Compiler, Linker

Assembly-language programming:

Addressing Modes: direct, immediate, register, register indirect, indirect, base-register,

PC-relative, indexing

Instruction/Machine cycle

Instruction-set Design Issues: which instructions to include (#, complexity), which built-in data types, instruction format [length (fixed, variable), number of address (2, 3, etc), field sizes], # registers, addressing modes supported

Chapter 12. CPU

General CPU organization: general purpose (user-visible) registers, control & status registers (PC, IR, MAR, MBR, PSW), ALU, control unit, internal CPU bus

Instruction cycle

Pipelining:

pipeline registers - purpose

Pipeline stalls/delay causes:

1) structural hazards (i.e., piece of hardware needed by several stages at the same time)

2) data hazards (i.e., need a value before it is calculated) and bypass signal paths/forwarding to minimize

3) branch delays (i.e., fetch wrong instructions before you either know it is a branch instruction or the outcome of the branch is known)

Ways to reduce the branch penalty: multiple streams, prefetch branch of target, loop buffer, branch prediction, and delayed branch

Branch History Table - 1-bit (last outcome as prediction) and 2-bit (need to be wrong twice to change your prediction)

Chapter 13. RISC

CISC vs. RISC - motivation and characteristics of each

General understanding of why a CISC is hard to pipeline

Use of large register files - register windows

register file vs. cache

Chapter 14. ILP and Superscalar Processors

Superpipelining - MIPS architecture

Superscalar characteristics

Instruction-level parallelism and its limitations due to write-read/RAW data dependencies, procedural dependencies, and resource conflicts.

Machine-level parallelism

Instruction-issue policies: In-order Issue with In-order Completion, In-order Issue with Out-of-Order Completion, and Out-of-Order Issue with Out-of-Order Completion

Dependencies: true data dependencies (read-after-write/RAW), output (write-write/WAW) dependencies, antidependencies (read-write/WAR)

Instruction window, Register renaming, Tomasulo's algorithm

General understanding of the Pentium 4 pipeline (DON'T memory stages, but just try to get the general concepts)