

Test 2 is Thursday, November 12. You will be allowed one 8.5" x 11" cheat sheet of notes (you can use the front and back of the page).

Chapter 3. (Mostly Sections 3.3 to 3.7)

Bus interconnection: shared collection of wires with lines classified as data, addr., control

Steps of a typical bus transfer

Types of buses: system bus, backplane bus, multiple bus hierarchies

Elements of bus design: 1) dedicated/(time) multiplexed, 2) centralized vs. decentralized arbitration, 3) synchronous vs. asynchronous timing, 4) bus width

PCI bus protocol

Digital Logic Review (no direct questions from this material) (You can also see Stallings on-line chapter 20 at: <http://williamstallings.com/COA/COA8e.html>)

Common combinational circuits: decoder, multiplexer (MUX)

Sequential Circuits (Memory): SR latch - know how it remembers (two stable states, etc.), know how it changes states;

Clocked Flip Flops: SR flip flop, D Flip flop, etc.; their characteristic tables
register file - design and usage

Chapter 4. Cache Memory

Memory hierarchy: levels and goals (speed, capacity, and cost)

Key characteristics of memory - table 4.1

Performance: access time, memory cycle time, transfer rate

Locality of reference (temporal and spatial)

Idea of cache (and virtual memory)

cache: type (direct mapped, fully associative, set associative); replacement algorithms; write policies (write-through, write-back); cache-coherency solutions; block size; number/level of caches; unified vs. split cache

Chapter 5. Internal Memory

RAM: static (SRAM) and dynamic (DRAM)

Square-memory design of RAM

Error Correction: single-error correction using Hamming Code,

Advanced DRAM Organizations: Synchronous DRAM (mainly)