Computer Architecture Fall 2009

Lect #	Tuesday		Thursday	
1	8/25	Ch. 2: High-level and Assembly Language Review (NULL: Sections 4.8 - 4.12)	8/27	Ch 10 & 11: Instruction Sets (NULL: Sections 5.1-5.4; 9.1-9.2)
3	9/1	Ch. 12: Instruciton Pipelining NULL: Section 5.5)	9/3	Ch 12: Pipeline Data Hazards and Forwarding
5	9/8	Ch 12: Pipeline Branch Hazards (NULL: Section 11.5)	9/10	Ch 13: RISC vs. CISC (NULL: Sections 9.1-9.2)
7	9/15	Ch 14: Instruction-Level Parallelism (ILP) and Superscalar Processors (NULL: 9.3 - 9.4.1)	9/17	
9	9/22	Ch 14: ARM Cortex-A8 Processor	9/24	
11	9/29	Review for Test 1	10/1	**Test 1**
13	10/6	Ch 3: Bus Design Issues (NULL: Section 4.3 and 7.5)	10/8	PCI Bus Protocol (NULL: Section 13.5.3)
15	10/13	Ch 5: Memory Hierarchy (NULL: Section 6.1 – 6.3)	10/15	
17	10/20	Ch 4: Cache Memory (NULL: Section 6.4)	10/22	Ch 5: RAM/Main Memory (NULL: Section 4.6 and 3.6.5)
19	10/27	Ch 6: Magnetic Disks and RAID (NULL: Sections 7.6, 7.9-7.10)	10/29	Ch 7: I/O: memory-mapped vs isolated I/O; programmed-I/O, interrupt-driven, and DMA (NULL: Sections 7.1-7.4)
21	11/3	Review for Test 2	11/5	**Test 2**
23	11/10	Ch: 8: Operating System Support (NULL: Chapter 8)	11/12	Ch 8: Virtual Memory (NULL: Section 6.5)
25	11/17	Ch 8: Page replacement, page allocation, and segmentation	11/19	Ch 17: Parallel Processing (NULL: Sections 9.3 - 9.6)
Thanksgiving Break: Nov. 23 - 27				
27	12/1		12/3	Ch. 18: Multicore Computers
29	12/8		12/10	Review for Final