Computer Architecture (810:142), Fall 2010

Time and Place: 2:00 AM to3:15 PM Tuesday and Thursday in ITTC 328

Web-site: www.cs.uni.edu/~fienup/cs142f10/

Class Email List: Send messages to 810-142-01-FALL@uni.edu from your UNI account (let me know other email addesses that you want to use)

Instructor: Mark Fienup (fienup@cs.uni.edu)
Office: ITTC 313
Phone: 273-5918 (Home 266-5379)
Office Hours: M 9-11, 1:10-3; T 9:30-10:30; W 1:10-3; Th 9:30-10:30; F 9-11, 1:10-3

Prerequisite: Computer Organization (810:041)

Required Text: *Computer Organization and Architecture: Designing for Performance*, Eighth edition, William Stallings, Prentice Hall, 2010**.** ISBN-10: 0136073735 ISBN-13: 9780136073734

Course Goals: Very few people will become computer architects, but the vast majority of students will be employed as a software "somethings" (software engineer, software tester, programmer, etc.). Unfortunately, efficient software systems can only be produced by people with a thorough understanding of computer hardware and its relationship to software. Therefore, the major goal of this course is to understand the relation between the hardware and software, and how to efficiently use the hardware. To achieve this you will learn about (1) the hardware organization of sequential and parallel computers, (2) the memory hierarchy including cache and virtual memory, (3) system I/O and communication, (4) interrupts, (5) hardware support for operating systems, and utilitization of mult-core processors & many-core GPUs.

Assignments: The majority of your assignments will be "pencil-and-paper" exercises. However, we might have an occasional programming assignments to highlight the importance of understanding the computer architecture when designing and writing software.

Pedagogic Approach: In class, I'll tend to break up the lecture with active (and group) learning exercises to aid learning. While this is not formally graded, part (5%) of your grade will be based on your participation on these in-class activities. Students benefit by (1) increased depth of understanding, (2) increased comfort and confidence, (3) increased motivation, and (4) being better prepared to work in groups on the job. This might sound great, but it will require you (and me) to work differently to prepare for class. Before the class, you must read the assigned reading, thought about what I've asked you to think about, etc.; otherwise you won't be able to effectively participate in your group during class.

Grading policy: There will be three tests (including the final). I'll announce tests at least one week in advance to allow you time to prepare. Tentative weighting of course components is:

In-class Work:	5 %	
Assignments:	25 %	
In-class Test 1:	23 %	(about Sept. 30)
In-class Test 2:	23 %	(about November 4)
Final:	24 %	(Wednesday, December 15 from 1-2:50 PM in ITT 328)

Grades will be assigned based on straight percentages off the top student score. If the top student's score is 92%, then the grading scale will be, i.e., 100-82 A, 81.9-72 B, 71.9-62 C, 61.9-52 D, and below 52 F. Plus and minus grades will be assigned for students near cutoff points.

Special Notice: In compliance with the University of Northern Iowa policy and equal access laws, I am available to discuss appropriate academic accommodations that may be required for students with disabilities. Requests for academic accommodations are to be made during the first three weeks of the semester, except for unusual circumstances, so arrangements can be made. Students are encouraged to register with Student Disability Services, 103 Student Health Center, to verify their eligibility for appropriate accommodations.

Computer Architecture Schedule for Fall 2010

Lect #	Tuesday		Thursday	
1	8/24	Ch. 2: High-level and Assembly Language Review	8/26	Ch 10 & 11: Instruction Sets
3	8/31	Ch. 12: Instruciton Pipelining	9/2	Ch 12: Pipeline Data Hazards and Forwarding
5	9/7	Ch 12: Pipeline Branch Hazards	9/9	Ch 13: RISC vs. CISC
7	9/14	Ch 14: Instruction-Level Parallelism (ILP) and Superscalar Processors	9/16	Ch 14: ARM Cortex-A8 Processor
9	9/21	Ch 3: Bus Design Issues	9/23	Ch 5: Memory Hierarchy
11	9/28	Review for Test 1	9/30	**Test 1: Chapters 2, 10-14**
13	10/5		10/7	Ch 4: Cache Memory
15	10/12	Ch 5: RAM/Main Memory	10/14	Ch 6: Magnetic Disks and RAID
17	10/19	Ch 7: I/O: memory-mapped vs isolated I/O; programmed-I/O, interrupt-driven, and DMA	10/21	Ch: 8: Operating System Support
19	10/26		10/28	
21	11/2	Review for Test 2	11/4	**Test 2: Chapters 3 - 5, and Digital Logic**
23	11/9	Ch 8: Virtual Memory	11/11	Ch 17: Parallel Processing
25	11/16		11/18	Ch. 18: Multicore Computers
Thanksgiving Break				
27	11/30	Many-core Computing	12/2	
29	12/7		12/9	Review for Final Exam
Final: 1**-2:50 PM Wednesday, December 15 in ITT 328**				