

HW #4 Computer Systems
Due: 10/10/06 (T)

1. Draw and explain a timing diagram for a PCI write operation. Assume that 3 data transfers occur and that the following occurs during these transfers:

- during the first data transfer, the target is not ready for two clock cycles
- during the second data transfer the initiator is not ready for one clock cycles, and
- during the third data transfer, the target is not ready for two clock cycles.

You are to draw a diagram similar to Figure 3.23. On your diagram clearly indicate:

- the address and data phases and any wait states,
- which wire(s) are controlled by the target device, initiator device, or both, and
- when the data is read off the bus by the target.

2. Complete the below timing diagram for the following sequence of bus transactions:

- device A wants to do a read transfer and has asserted REQ A# at the start of cycle 0
- device B wants to do a read transfer and has asserted REQ B# at the start of cycle 0
- device C wants to do a write transfer and has asserted REQ C# at the start of cycle 0

Make the following assumptions:

- devices A, B, and C all only want to transfer one piece of datum
- the arbiter uses a round-robin priority scheme where currently Device B has the highest priority and device Device A has the lowest priority
- for all three data transfers, both the initiator and target are ready as soon as possible
- Before cycle 0 starts, the previous bus master deasserts IRDY# so it is free

The below figure shows the request (REQ#) and grant (GNT#) lines. Notice the hidden arbitration that PCI uses to hide arbitration.

