1) In Figure 3.19 (synchronous read), how was bus skew handled?

2) In Figure 3.20 (a) where the CPU is reading from Memory, which device is driving the wires:
   a) Status lines?
   b) Address lines?
   c) Read?
   d) Data lines?
   e) Acknowledge?

3) In Figure 3.20(a) (asynchronous read), how was bus skew handled?
4) How does a hierarchy of buses as shown in Figure 3.18 improve performance of a computer system?

5) What is the purpose of the “Bridge”s as shown in Figure 3.18?