

Team #: \_\_\_\_\_  
Absent:

**Solution**

Name: \_\_\_\_\_

1. In Figure 3.23 (PCI read operation), why is a turn-around cycle needed between the Address and Data on the AD lines?

Turn-around cycles are needed whenever one device stops driving(/using) a line and another device starts driving(/using) a line. On a read, Address is sent by the Initiator while the Data is sent by the Target, so a turn-around cycle is needed.

2. (see next page)

3. In the PCI protocol each device has its own set of dedicated bus arbitration lines. All of the arbitration lines go to a centralized arbitrator. Why does the PCI protocol **not** specify a specific arbitration scheme (such as first-come-first-serve)?

The designers of PCI wanted it to be used for a lot of applications. By not specifying a specific arbitration scheme PCI can be used in many situations.

4. How does a hierarchy of buses as shown in Figure 3.22 improve performance of a computer system?

Having many buses allows for each bus to be operating in parallel. A single bus system would be limited to one bus operation at a time.

Each bus in the hierarchy can be customized to needs of the devices using it. For example, the “System bus” in Figure 3.22 (b) would need to operate at a very high speed (faster than PCI), so it might be physically limited by its length to only a few connections.

5. What is the purpose of the “Bridge”’s as shown in Figure 3.22?

The “Bridge” connects two buses together. Since the buses are operating using different protocols and speeds, the bridge acts as a buffer and translator between the protocols.

Absent:

2. Draw and explain a timing diagram for a PCI read operation (similar to Figure 3.23). Assume that 2 data transfers occur and that the following occurs during these transfers:

- during the first data transfer the initiator is not ready for two clock cycles, and
- during the second data transfer the target is not ready for one clock cycle.

On your diagram clearly indicate:

- the address phase, data phase(s) and any wait states
- which wire(s) are controlled by the target device and which are controlled by the initiator device
- when the “target” reads the data off the bus

