The final will be 1-2:50 PM on Wednesday, May 7, in ITT 322. The test will be closed-book and closed-note, except for three sheets of paper with notes. About 70% of the Final will focus on the material since the last test, and about 30% will focus on tests 1 and 2 material.

Chapter 8. OS Support and Virtual Memory
OS objectives and functions
Effects of multiprogramming on system utilization
Process control block (PCB) components
Scheduling of jobs: types of queues and their purpose
Scheduling techniques, priorities, and fairness
Memory management: swapping, fixed partition and variable partitioning
Paging: virtual memory, demand paging, page table and virtual to physical address translation, time and memory efficiency considerations, TLB (translation lookaside buffer)
Handling of large page tables: two-level page table, inverted page table
Page-replacement algorithms and their implementation (R-bits & history bits)
Frame-allocation algorithms: page-fault frequency algorithm
Segmentation: advantages and disadvantages
Segmentation and paging combined

Chapter 18: Parallel Processing and Multiprocessor Systems (Power Point Presentations)
Introduction to Multiprocessors
Need for multiprocessors and clusters
Amdahl’s law
Trends in supercomputers (Top 500) toward clusters
Flynn’s Classification: SISD, SIMD, MISD, MIMD
Multitprocessor basic organizations: Communication models (message passing vs. shared memory(UMA, NUMA) and physical connection (network vs. bus)

Bus Connected Multiprocessors
Single bus multiprocessor issues: cache coherency, process synchronization, spin locks

Network Connected Multiprocessors
Network connected multiprocessors: message passing (sends & receives), cache coherency in NUMAs (directory-base protocols)
Interconnection network (IN) metrics: cost (# switches, links/switch, link width, link length), network bandwidth, bisection bandwidth, others (latency, throughput, # routing hops)
Interconnection network types: bus, ring, fully connected, crossbar, hypercube, 2D & 3D mesh/torus, fat tree
Network of Workstations (NOW) Clusters

Multicore processors
Performance issues related to the memory hierarchy, e.g., the need for data reuses
Current Multicore Problems: small caches, TLB not covering caches, memory bandwidth bottleneck
Motivation of multithreading on a chip: hide stalls due to dependency, cache misses, etc. and thus increase utilization of functional units
Types of multithreading on a chip: fine-grain, course-grain, simultaneous multithreading (SMT)