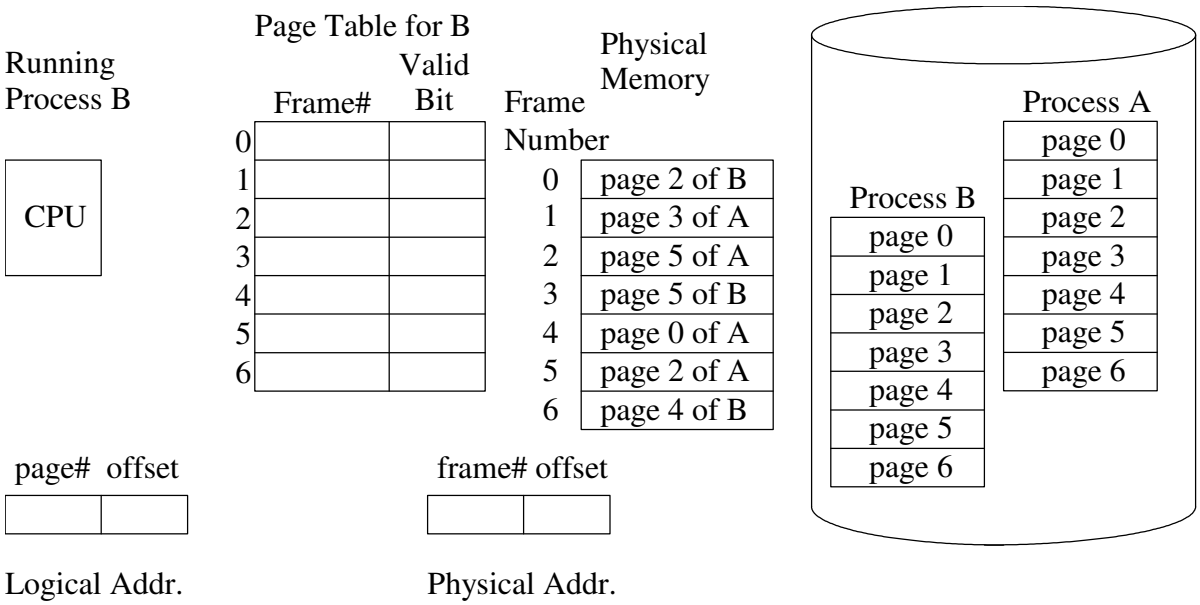
1. Consider the demand paging system with 1024-byte pages.



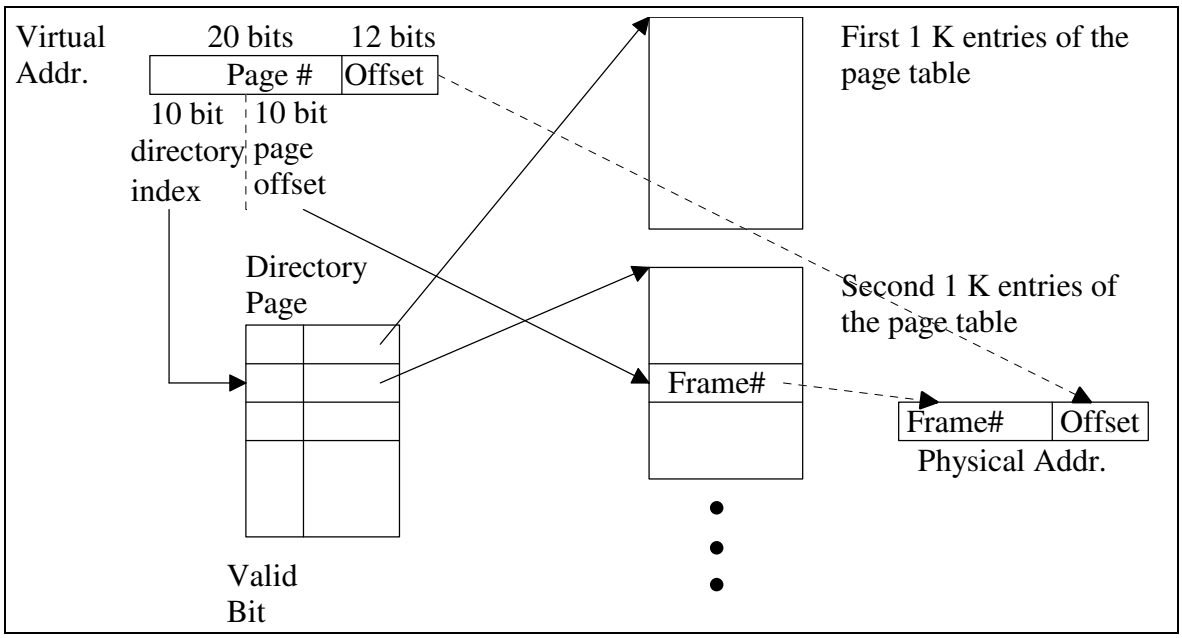
a) Complete the above page table for **Process B**.

b) If process B is currently running and the CPU generates a logical/virtual address of 2060_{10}, then what would be the corresponding physical address?

2. For a 32-bit address machine with 4 KB (2^{12} bytes) pages and 4 byte page-table entries, how big would the page table be?

3. How does a TLB (translation-lookaside buffer) speed the process of address translation?

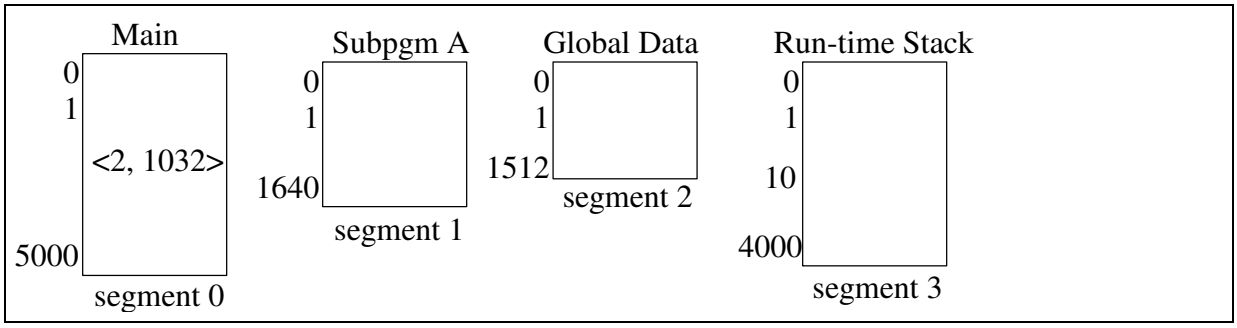
4. 32-bit computers typically had 4KB pages, 4 byte page table entries, and used two-level page tables where the first level (the "directory") acts as an index into the page table which is scattered across several pages.



A 64-bit computer might not support a full 64-bit address space. How could a 3-level page table support 42-bit address space?

5. If only segmentation was used, what problems would you predict with moving whole segments into and out of memory?

6. Assuming a page size of 1024 bytes, complete the Page Tables for the pages in memory, and determine the physical address for the logical address <2, 1032>.



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