Mark F.

Comp. Arch. Homework #1 Due: Friday (9/12) 3 PM

.5 1) How is a computer system protected from a user program that goes into an infinite loop?
CPU timer that traps to OS if it expires. It is settable by privileged instr.

.5 2) Assume special I/O instructions are used to fill I/O-controller registers. Why can't a user program use these instructions to communicate with the I/O device directly and "by-pass" the operating system's protection checking? I/O instr. are privileged so only system mode process can execute them

.5 3) Assume that memory-mapped I/O is used. Since Load and Store instructions are used to communicate with the I/O-controller registers, why can't a user program communicate with the I/O device directly and "by-pass" the operating system's protection checking? A user-pgm is restricted to its own addr. space by the MMU. The addr. of I/O controller reg. are outside its addr. space.

4) Suppose we had a block transfer from an I/O device to memory. The block consists of 2048 words and one word can be transferred at a time. For each of the following, indicate the number of interrupts needed to transfer a block:

1.0 a) programmed-I/O 0 - but wastes CPU time

b) interrupt-driven I/O 2048

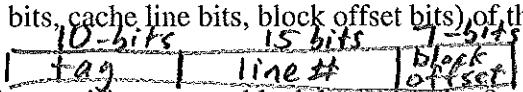
c) DMA (direct-memory access) - 1 after whole block transferred.

5) Suppose we have a 4 GB (2^{32} bytes) memory that is byte addressable, and a 4 MB (2^{22} bytes) cache with 128 (2^7) bytes per block.

a) How many total lines are in the cache? $\frac{2^{22}}{2^7} = 2^{15}$ lines

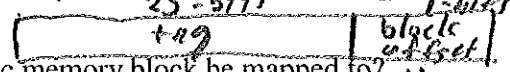
b) If the cache is direct-mapped, how many cache lines could a specific memory block be mapped to? 1

2.0 c) If the cache is direct-mapped, what would be the format (tag bits, cache line bits, block offset bits) of the address? (Clearly indicate the number of bits in each)



d) If the cache is fully-associative, how many cache lines could a specific memory block be mapped to? 2^{15}

e) If the cache is fully-associative, what would be the format of the address?



f) If the cache is 4-way set associative, how many cache lines could a specific memory block be mapped to? 4

g) If the cache is 4-way set associative, how many sets would there be? $2^{15}/2^2 = 2^{13}$ sets

h) If the cache is 4-way set associative, what would be the format of the address?

4.5