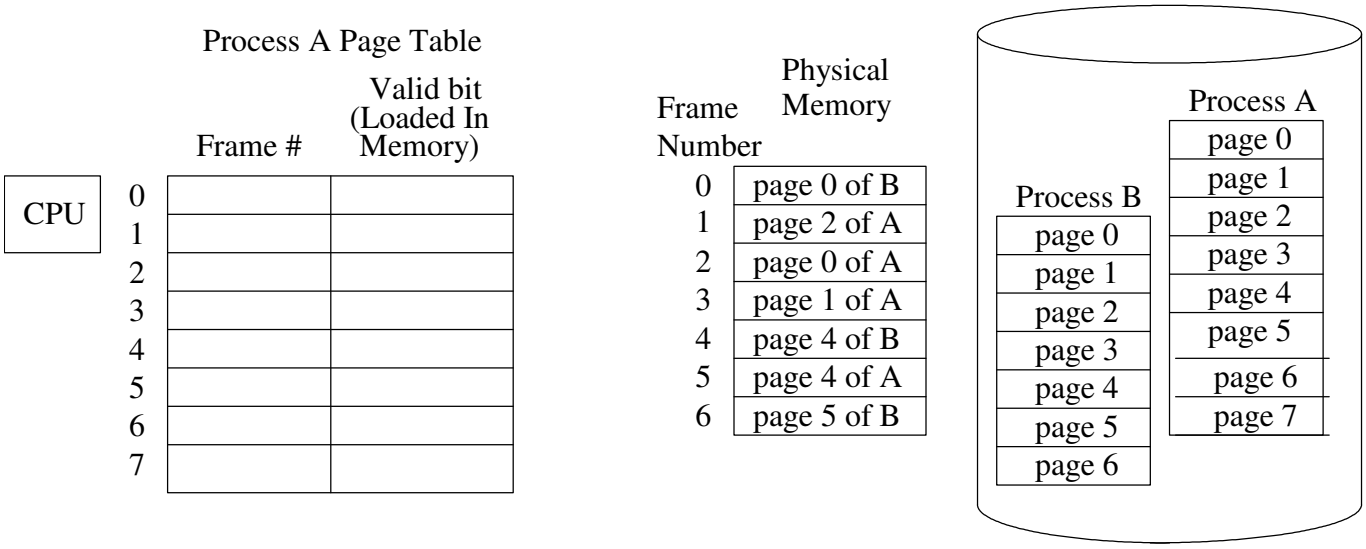
Fall 2008 Name:_____

Computer Architecture Test 2

Question 1. (7 points) There are many similarities between the cache-memory level and memory-disk level of the memory hierarchy, but there are also important differences. A cache miss stalls the running program temporarily, but a page fault causes the running program to turnover the CPU to another program. Why are these cases treated differently by the computer system?

Question 2. (10 points) Consider a demand paging system with 1024-byte pages.



a) Complete the above page table for **Process A**.

b) If process A is currently running and the CPU generates a logical/virtual address of 232_{10}, then what would be the corresponding physical address?

Question 3. (8 points) What is the TLB (translation-lookaside buffer) and why is it important for efficient operation of a paged, virtual memory system?

Question 4. (9 points) For each type of virtual memory scheme and characteristic, indicate **T** (TRUE) if the virtual memory scheme has that characteristic; otherwise indicate **F** (FALSE).

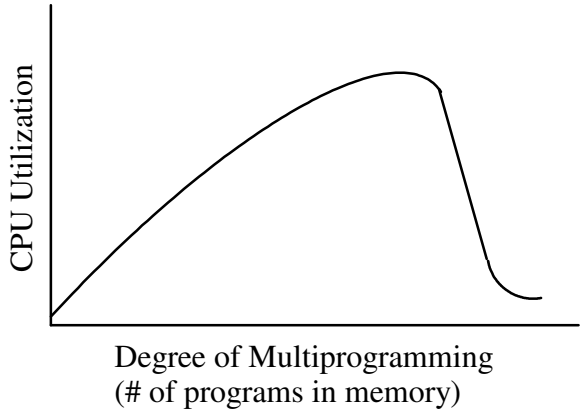
Characteristic	Paging Only	Segmentation Only	Combined Paged of Segments
Has fragmentation of main memory			
Uses fixed-partitioning of main memory			
Would benefit by a translation-look-aside buffer (TLB)			
Would benefit by a cache (holding memory blocks)			
Can protect logical parts of the program (main pgm, subpgms, run-time stack, global variables, etc.) separately			
Allows a program to execute eventhough it is only partial loaded in main memory			

Question 5. (6 points) How many page faults would occur for each of the following page replacement algorithms. Assume 3 page frames are allocated to the process.

Optimal: Reference string - 1 2 4 5 1 2 3 4 5 1 2 3

LRU: Reference string - 1 2 4 5 1 2 3 4 5 1 2 3

Question 6. (8 points) Below is the expected plot of "CPU Utilization" vs. "Degree of Multiprogramming" on a paged, virtual-memory computer system. Explain why the CPU utilization grows nearly linearly during the rising part of the curve.



Question 7. (5 points) To approximate the LRU page-replacement algorithm, a hardware maintained reference (R) bit and history bits can be stored for each entry in the page tables. Periodically, say every 10 milliseconds, an interrupt causes the OS to shift the R-bit into the counter/history bits.
Consider the following snapshot of R-bits and couter/history bits.

	R	Counter/History bits
page 0	0	0 0 1 1 0 1 0
page 1	1	0 0 1 0 0 0 0
page 2	1	0 1 0 1 0 1 0
page 3	0	0 0 0 1 1 1 1
page 4	1	0 0 0 0 0 1 0

a) If a page fault occurs, which page should be selected for replacement?

b) How long has it been since page 0 has been referenced? (give a range)

Question 8. (6 points) Suppose we had a block transfer from an I/O device to memory. The block consists of 2000 words and one word can be transferred to/from memory at a time. For each of the following, indicate the number of interrupts needed to transfer a block using:

a) DMA (direct-memory access)

b) interrupt-driven I/O

c) programmed-I/O

Question 9. (9 points) On a **paged, multiprogrammed, multi-user** computer system that has isolated-I/O (separate I/O) instructions, describe what hardware support for the operating system is needed to:

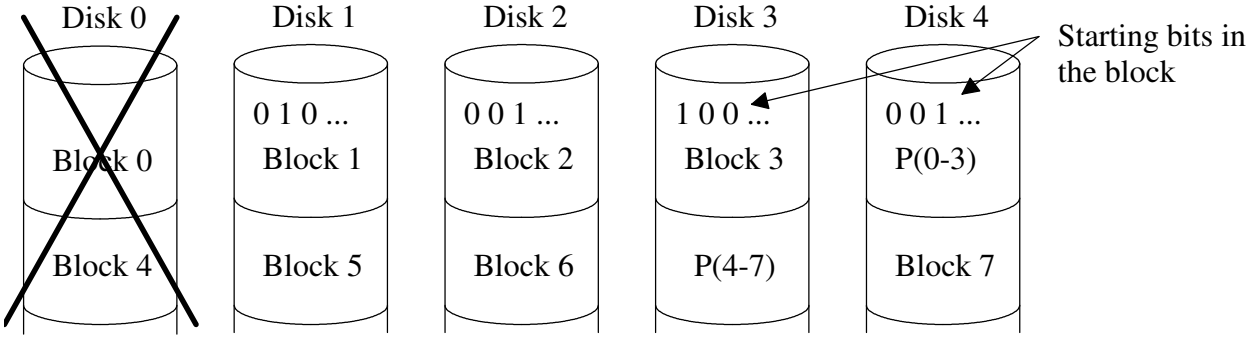
a) guard against infinite loops in user programs

b) restrict a user program to its own main memory address space

c) restrict a user program from accessing other users' data files

Question 10. (10 points) Suppose we have a 5 disk RAID 5 (block-level distributed parity) array.

a) If Disk 0 crashes, reconstruct the first three bits of block 0. Assume even parity is being used.

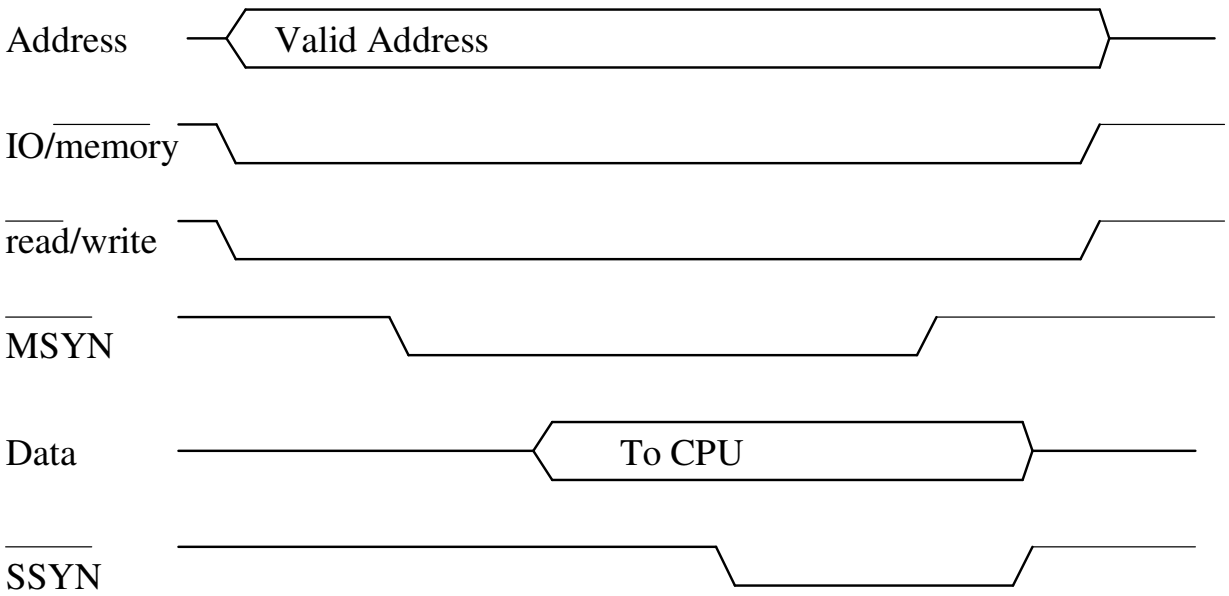


b) Assume that Disk 0 has crashed. If you write a new block of data starting with bits 0 0 1 ... to Block 3, then can Blocks 1 and 2 be read at the same time as the write for Block 3 is occurring? (Justify your answer)

Question 11. (8 points) Suppose we have an 6 disk RAID array with each disk having a 100 MB/sec data transfer rate. Complete the following table **assuming ONE of the disks is faulty.**

RAID Level	Maximum number of concurrent, independent READs	Maximum number of concurrent, independent WRITEs	Data Transfer Rate for a single large READ
RAID 0 (no redundancy with **large strips**)			
RAID 1 (Mirroring with **large strips**)			
RAID 3 (bit-interleaved parity)			
RAID 5 (block-level distributed parity)			

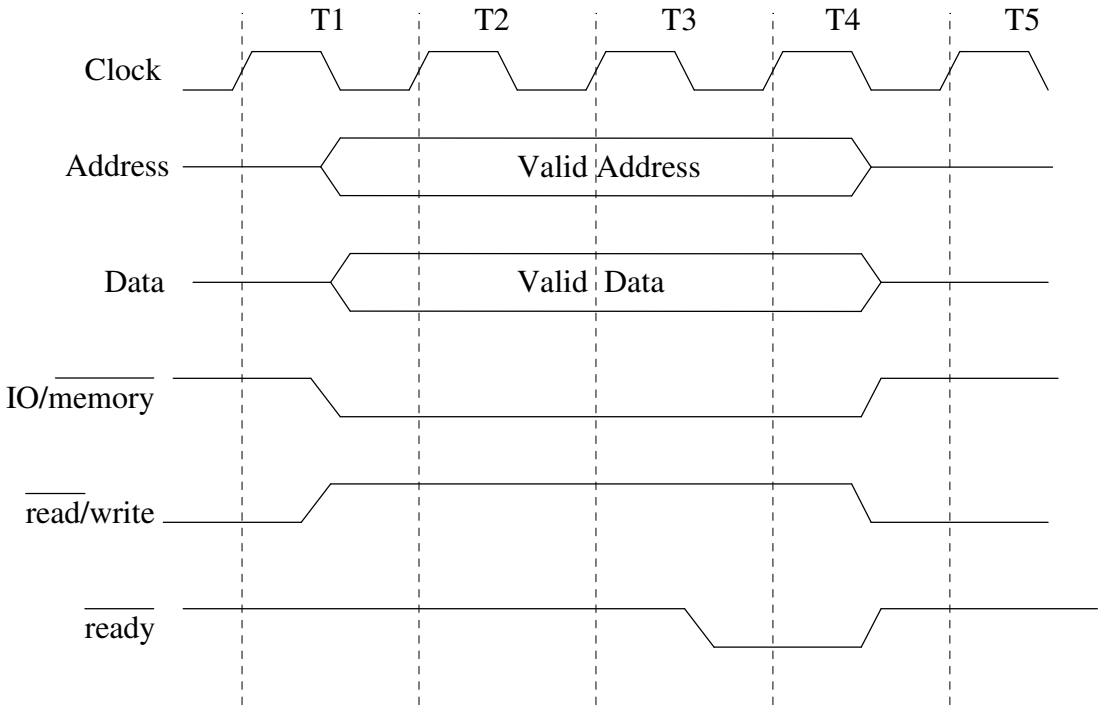
Question 12. (7 points) Consider the asynchronous READ timing diagram.



a) How does the CPU know that the data is available on the Data lines?

b) How is bus skew handed?

Question 13. (7 points) Consider the CPU doing a synchronous memory write operation with one wait states.



a) Indicate which wires are controlled by the CPU and which are controlled by the memory.

b) When (in clock cycles) is the data read off of the Data wires?

c) Why do devices change the values being sent in the middle of the clock cycles, and read the values on the start of the next clock cycle?