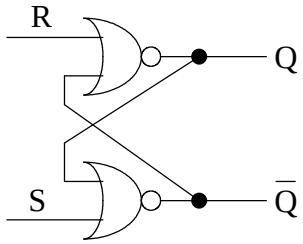
Team #:____ Name:_____
Absent:

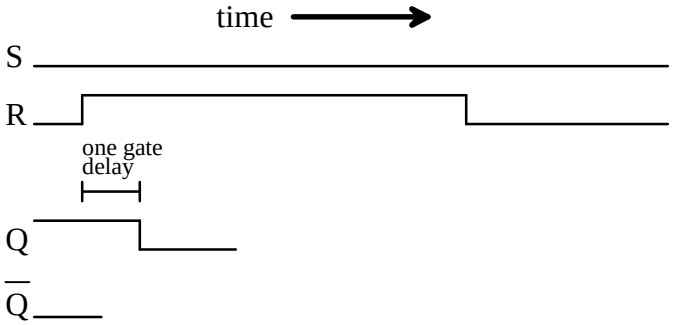
1. a) If R = 0 and S = 1, then what will be the output on Q and $\overline{Q}$?



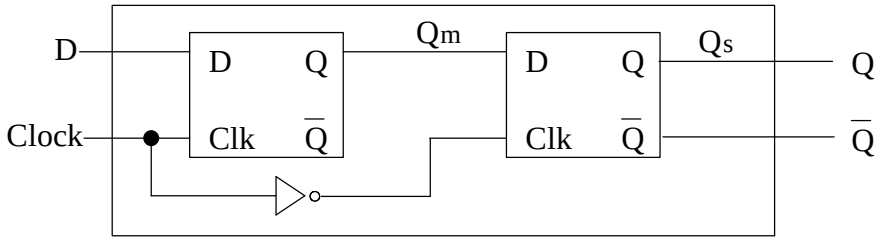
A	B	$\overline{(A+B)}$
0	0	1
0	1	0
1	0	0
1	1	0

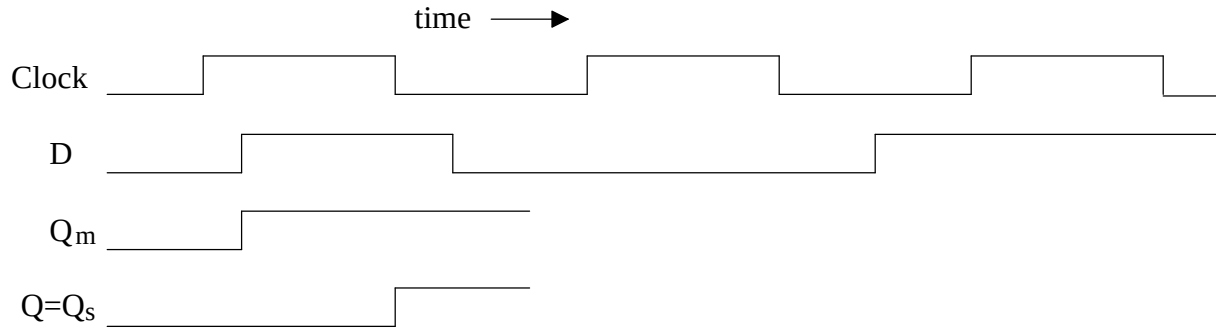
b) Now, if S goes to a 0 value, what happens to the output on Q and $\overline{Q}$?

c) Complete the following timing diagram for the SR latch:



2. Complete the following timing diagram for the Master-Slave D flip-flop:





Team #:____ Name:_____
Absent:

3. Suppose we have a register file with the following specifications:
- 16 registers numbered from 0 to 15
- each register has 32-bits
- one write port
- two read ports

a) What how many bits(/"wires") would be need for each of the following?
- data to be written for a write port
- specifying the register number of a read port
- specifying the register number of a write port
- output read from a read port

b) How many write enable wires would be needed for the whole register file?

c) How many decoders would be needed in the implementation of the whole register file (Figure B.8.9)? Explain how you arrived at that number and specify the type of decoders (i.e., number of inputs and number of outputs for each decoder)

d) How many multiplexers would be needed in the implementation of the whole register file (Figure B.8.8)? Explain how you arrived at that number and specify the type of multiplexers.

4. Suppose we have a 32 word memory.
a) How many bits would be needed for the binary address?

b) What would be the range of binary addresses?

c) If we wanted to group four words together into a block and number the block starting at zero (i.e., block 0 consists of addresses 0, 1, 2, 3; block 1 consists of addresses 4, 5, 6, 7, etc.), then what would be similar about the (binary) addresses of all the words within the same block?

5. Consider scaling the register file design (Figures: B.8.8 and B.8.9) to memory sizes. If we scaled up this design to 4 M x 4 (2^{22} words of 4-bits each), then:
a) How many total gates would be needed to implement the decoders?

b) How many total gates would be needed to implement the MUXs?

c) Assuming 5 gates per bit of memory, compare the number of gates needed to store the memory values with the number of gates need for overhead (gates for the decoder and MUX(s))?