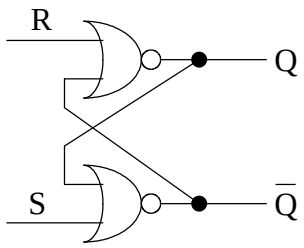
Team #:____ Name:_____
Absent:

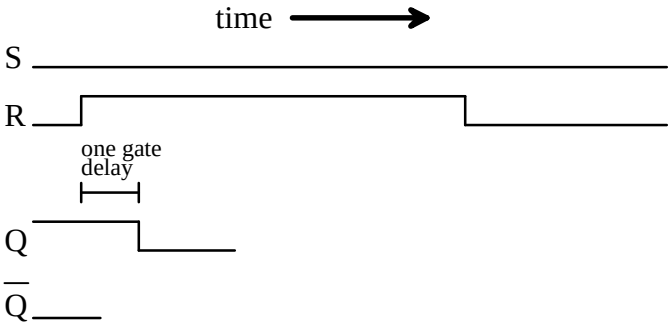
1. a) If R = 0 and S = 1, then what will be the output on Q and $\overline{Q}$?



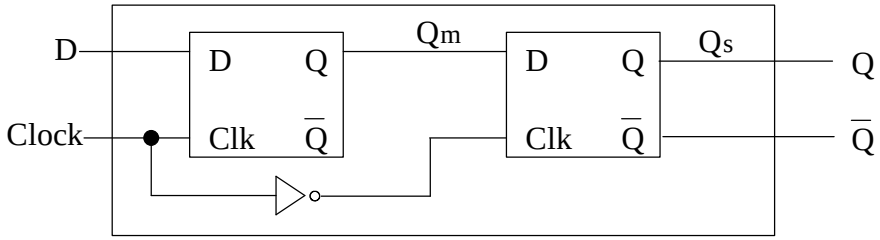
A	B	$\overline{(A+B)}$
0	0	1
0	1	0
1	0	0
1	1	0

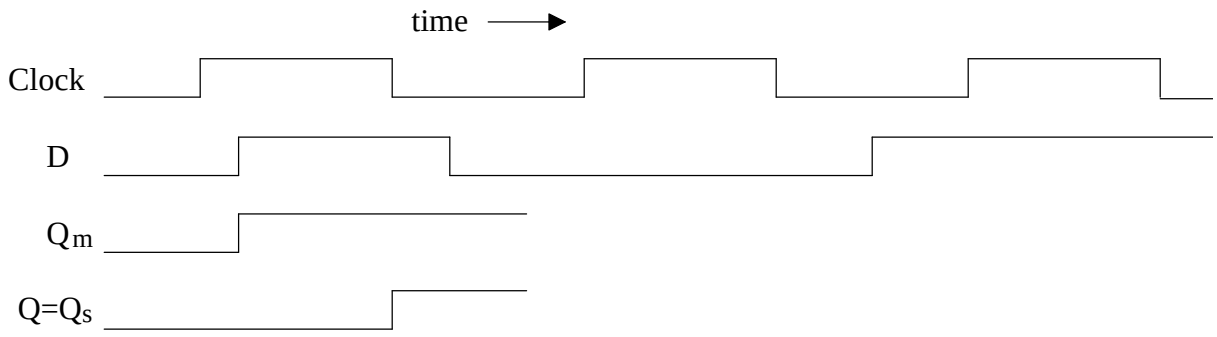
b) Now, if S goes to a 0 value, what happens to the output on Q and $\overline{Q}$?

c) Complete the following timing diagram for the SR latch:



2. Complete the following timing diagram for the Master-Slave D flip-flop:





Team #:____ Name:_____
Absent:

3. Suppose we have a register file with the following specifications:
- 8 registers numbered from 0 to 7
- each register has 16-bits
- one write port
- two read ports

a) What how many bits(/"wires") would be need for each of the following?
- data to be written for a write port
- specifying the register number of a read port
- specifying the register number of a write port
- output read from a read port

b) How many write enable wires would be needed for the whole register file?

c) How many decoders would be needed in the implementation of the whole register file (Figure B.8.9)? Explain how you arrived at that number and specify the type of decoders (i.e., number of inputs and number of outputs for each decoder)

d) How many multiplexers would be needed in the implementation of the whole register file (Figure B.8.8)? Explain how you arrived at that number and specify the type of multiplexers.

4) Complete the below diagram of a 4-bit register so that it is able to perform the following operations:
- parallel read/output of all bits (just look at the Q values)
- parallel write/input of all bits
- logical shift left one bit position (value shifted out of most-sign.bit is lost and a "0" is shifted into the least-significant bit)
- circular shift right one bit position (value shifted out of least-sign. bit is shifted into the most-significant bit)
- arithmetic shift right (sign-extend the most-significant bit)