Message

110011001101

Placeholder bits 0000

Generator

CRC
Cyclic Redundancy Check

Sending computer calculates the remainder bits 1011

CRC Redundancy bits to add to the message

4 redundancy bits for the 5 bit generator
The diagram illustrates a process involving a generator and a message, along with redundancy bits. Here's a breakdown:

1. **Generator**:
   - The generator is represented as 11001.

2. **Message**:
   - The message is represented as 11001100110.

3. **Redundancy Bits**:
   - Redundancy bits are added to the message, resulting in a new sequence: 110011001101011.

4. **Receiving Computer**:
   - The receiving computer gets the message and redundancy bits.

5. **Checking for Errors**:
   - The receiving computer uses the same generator to check for errors.
   - The process involves dividing the message and redundancy bits by the generator (11001).

6. **Remainder**:
   - The remainder obtained from the division is compared to a predefined value (0100).

7. **Verification**:
   - If the remainder matches the predefined value (0100), the message is considered error-free.
   - If the remainder does not match, it indicates an error in transmission.

8. **Final Verdict**:
   - If all data is correct, the message is considered valid.
   - If any error is detected, the message is discarded.